National Aeronautics and Space Administration

Qualified Electronics For Low Temperature Environments

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Program: Strategic Initiative

Project Objective:

Commercial off-the-shelf (COTS) electronics tend to have hidden margins enabling them to operate beyond datasheet limits. However, very little characterization & reliability results are available. Our objectives are to:

1. Develop a method for characterization and modeling of performance & reliability for COTS in extreme cold environments (-55C to -185C) of interest such as Europa, Titan, Mars nights, & Lunar nights
2. Establish a library of candidate parts, based on their characterization, literature data and technology.
3. Demonstrate the methodology by building and testing a cold functional assembly of cold-capable COTS selected based on technology info and characterization data.

Problem Statement

Current spacecraft architecture utilizes one or more central electronics box which require significant cabling increasing complexity and weight as demonstrated by this picture of the MER rover electronics at thermal-vac testing.

Cold capable electronic can enable electronics to be distributed on the extremities of the spacecraft next to sensors and motors, but currently there exists very few electronics components designed to operate in extremely cold temperatures.

Key Deliverables

FY 17:
- Demo subsystem selected for building with cold capable COTS
- Technology/literature analysis to identify key candidates
- Check out testing to narrow down candidates completed
- Initial development of behavior model for an example ADC part

FY18:
- 24 hour dwell test for candidate parts to demonstrate cold operability
- Refinement of initial ADC behavioral model with 24 hour dwell test data to enhance predictive capability and extending to second ADC

FY19:
- Complete 24 hour dwell test for remainder components
- Build pathfinder subsystem utilizing cold capable components
- Demonstrate cold operability for the pathfinder subsystem in the extreme cold environment.
- Complete cold-capable technology/parts pre-selection guideline with library of parts with literature data
- Complete universal ADC model for cold temperatures demonstrated on multiple ADCs of various architectures

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Benefits to NASA and JPL (or significance of results):

Many high value targets in the solar system require exposing the spacecraft to extremely low temperature environments, but current spacecraft architecture for such extreme environments rely on central warm boxes requiring significant routing cabling which increase complexity and weight. Alternatively, there exists very few electronics specifically designed for extreme cold operation. Therefore, this R&TD task was conceived as a pathfinder for the identification and qualification of commercial components for extreme cold environments (-55C to -185C) to support future NASA and JPL missions.

Upon completion of the three stated objectives, we would have developed, demonstrated and provided hardware evidence of an electronic subsystem assembly capable of functioning at extreme cold environments built from selected COTS components.

Additionally, we would have created infrastructures upon which additional electronics can be pre-selected to be qualified for operation in such environments.

FY19 Results:

- In preparation for building a full cold operation capable subsystem, we completed 24 hour sustained cold operation tests at -180C for the COTS parts needed in the full-board design, demonstrating their cold operational capabilities. For each part number, at least three parts were tested to establish statistical variation and demonstrate capability.
- The universal behavior/macro-model of CMOS Nyquist-rate analog to digital converters was refined using new test data with 24 hour dwell.
- ADC model's track-and-hold and quantization block diagrams were created in Matlab, separating the analog and digital components of the model. The model can be run by utilizing only datasheet information with minimal effort. An INL curve extraction tool is also provided.
- Final demo board assembled from the COTS-capable parts was tested at -180C. Final revision improved system performance, including noise and signal integrity. Board behavior was monitored to compare to RT results. Overall, the assembly performed well in cold, with all the critical ADC parameters staying within 0.5% of their room temperature values. Digital currents varied more than analog ones but everything remained operational throughout.
- A Wiki page was created for cold-tested part types, including FPGAs, op-amps, ADCs, discretes, passives and others, with downloadable resources from papers, publications and presentations hosted on the site. These parts were tested at NASA centers, universities and other related institutions. Wiki access link: **https://wiki.jpl.nasa.gov/display/parts/Cold-Tested+Parts+Library+and+Resources**

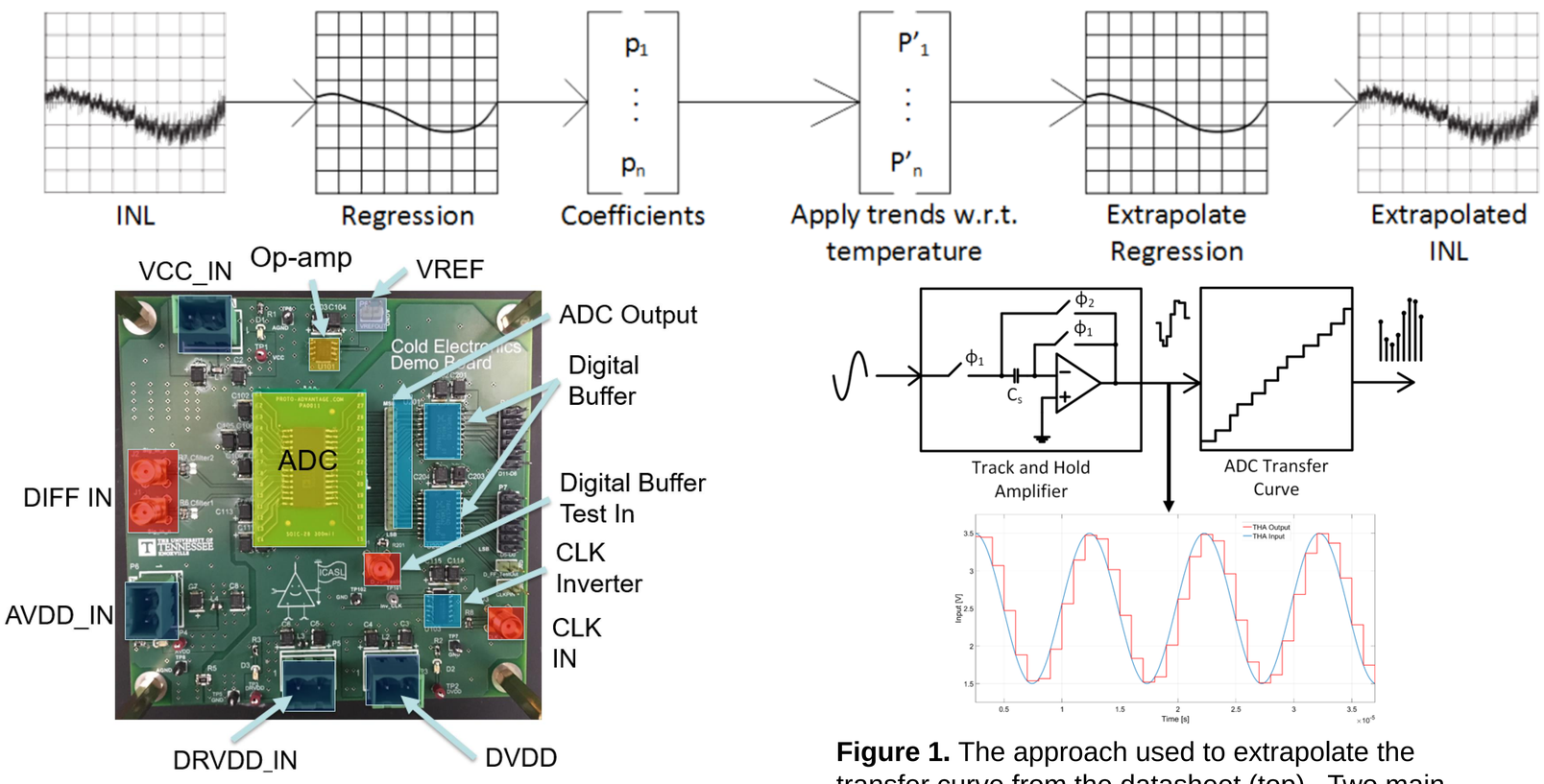

Figure 2. Final Demo Board Overview. Current revision improved the performance of the system, including noise and signal integrity.

Figure 1. The approach used to extrapolate the transfer curve from the datasheet (top). Two main components of model: THA parameters estimated, then INL curve for the transfer function is found.

	Part Type	Part Number	Type/Technology	Test Type	Lowest Test Temp. (°C)	# of Parts Tested	Test Institution	Resource Title	Resource Document	Comments
1	DC-DC	1003S12HN	10W Single Output Power Supply Module DC/DC Converter	Static	-180	1	NASA GRC	Evaluation of COTS SiGe, SOI, & Mixed Signal Electronic Parts for Extreme Temperature Use in NASA Missions	0930 - Reliability of SiGe, SOI, and Advanced Mixed Signal Devices for Cryogenic Space Missions.pdf	Oscillations in input current at -140°C under heavy loading.
2	Voltage Regulator	1003S12HN	Buck	Dynamic	-180	1	See paper	COTS IC Parts Pre-Selection Guideline for cryogenic applications	coldguideline-part2-rev2-0924.docx	Oscillation in input current observed at 133 K under heavy loading.
3	Passive Component	200B104KT50XT	BX Ceramic Capacitors	Dynamic	-185	3	NASA JPL	Reliability Final Report for Passive Components, ADC, FPGA: Cryogenic Testing	ArmianHanelli_FinalReport.pdf	This capacitor performed the worst with value drops of about 70% and is not recommended for use.

Figure 3. A sample of the Wiki page showing 3 part types, related information and resources.

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FY19 Publications

[A] Will Norton, Ziming Wang, Benjamin J Blalock, Jean Yang-Scharlotta, Mireyong Song, Mohammad Ashtijou, and Mohammad Mojarradi, "Modeling of Select Mixed-Signal Electronics for Cold Temperature Environments," *Proceedings of IEEE Aerospace Conference 2019.*

[B] Will Norton, Ziming Wang, Benjamin J Blalock, Jean Yang-Scharlotta, Mireyong Song, Mohammad Ashtijou, and Mohammad Mojarradi, "Testing and Modeling of a SAR ADC for Cryogenic Applications," *Proceedings of 2019 IEEE International Midwest Symposium on Circuits and Systems.*

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