National Aeronautics and Space Administration

# Rad-tolerant Low Power Avionics for Deep Space Small Spacecraft

**Principal Investigator: William D, Whitaker, Flight Electronics (349)**

**Tim Canham, Flight Software and Avionics Systems (348), Mike Pugh, Flight Communications Systems Section (337),**

**John O. Elliott, Project Systems Engineering and Formulation Section (312)**

**Program: Strategic Initiatives**

## Task Objective:

### Develop Low-SWaP-C flight avionics for small spacecraft

This task was focused on the development a low Size Weight, Power and Cost (SWaP-C) integrated avionics platform for small spacecraft applications. The objective is to develop software and hardware to mature the platform TRL5.

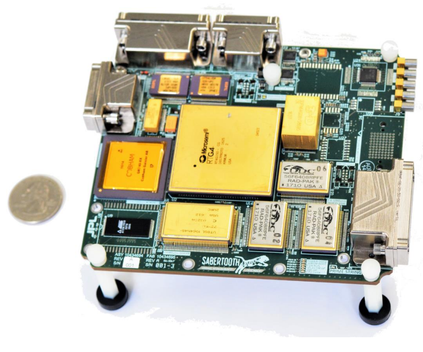
## Overall Objectives:

- Enable new missions order of magnitude improvement in SWaP-C
- Increase performance to meet the demands of future exploration
- Increase flexibility of spacecraft to enable more exotic and audacious missions.

## FY19 Results:

This year core functionality was developed in software and hardware:

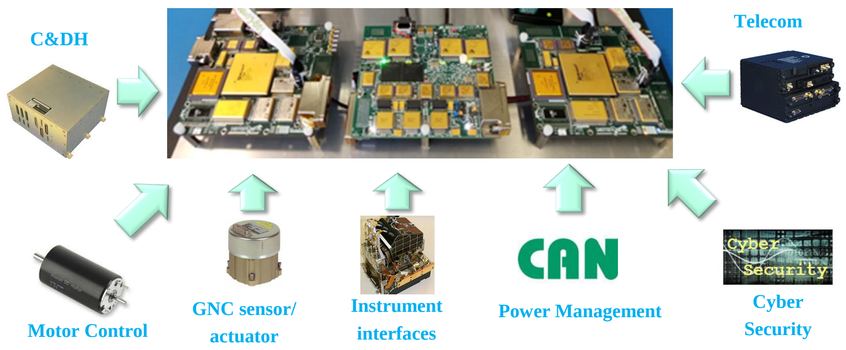
- Adaptive Fault Detection Unit and support for graceful degradation to make autonomous decisions to determine the stable conditions which allow spacecraft avionics to remain operational
- Compute on demand allowing the flight computer to power/depower autonomously to scale the power profile to the computational need throughout the mission phases.
- Port of UST radio to identify constraints and requirements for signal processing function for UST-lite
- Implementation of precision time distribution
- Demonstration of Initial Partition Loader, boot loader, operating system




## *Sabertooth Processor: integration of multiple subsystems*

**Sabertooth Avionics integrates multiple subsystems into a compact assembly**

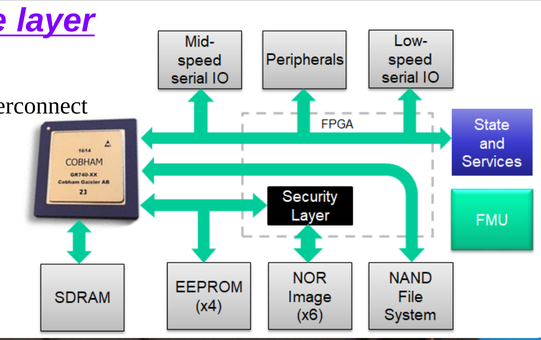
- Combine traditionally individual subsystems
  - CDH, telecom, Motor Control, GNC, power regulation/switch/housekeeping
- Integrate the functions of consistently-required support cards

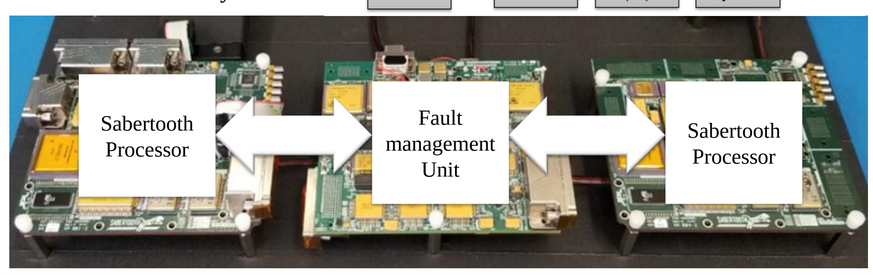



| Feature | Target |
|---|---|
| Processor | GR740 SPARC V8 Processor |
| Processor performance | 1200MIPS |
| Processor cores | Quad-Core |
| Power | 3W+ (Load dependent) |
| Mass | 2kg |
| Size | 11cm x 12cm |
| Radiation (Overall) | 100krad |
| Radiation (CPU) | 300krad |
| FPGA Device | Microsemi RTG4 FPGA |
| Board Supply Voltage | 5V |
| Data Storage | 8 GBytes NAND |
| Flight Software Storage | 6 X 32 Mbytes NOR |
| Start-up ROM Size | 4 x 64 kBytes with EDAC |
| RAM | 256MBytes PC100 SDRAM |
| SpaceWire | 8 Channels |
| Motor Control | 64 channels |
| GNC | 7 channels |
| Time distribution | 64 channels |
| Telecom | Full Iris transceiver signal processor + DAC/ADC |
| Packaging | Slice-based, Serial interconnect |

## *Sabertooth Compute layer*

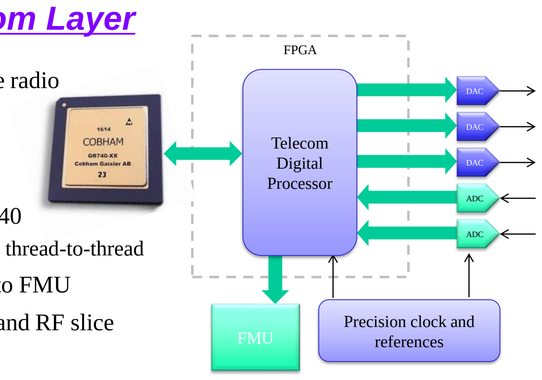
- GR740 Processor
- Spacewire for payload and interconnect
- Low-speed serial
  - SPI / UART / LVDS
- EEPROM bootloader
- FSW image memory
  - Cybersecurity protected
- NAND-based file system




## *Sabertooth Telecom Layer*

- Integrated Iris deep-space radio
  - Signal Processing
  - ADC/DACs
  - EMI doghouse in frame
- Radio FSW runs on GR740
  - Radio-CDH interface is thread-to-thread
- Radio firecode interface to FMU
- Supports UHF/X/S/Ka-band RF slice



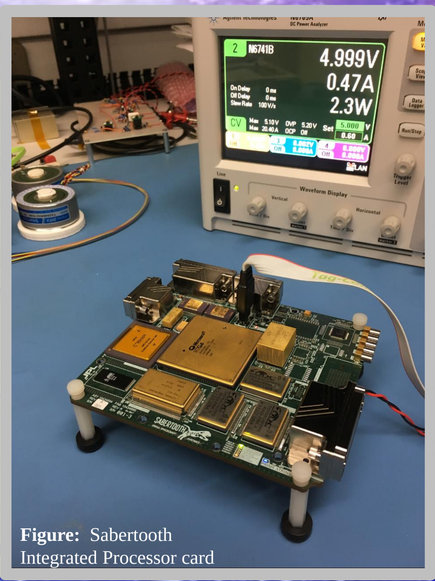
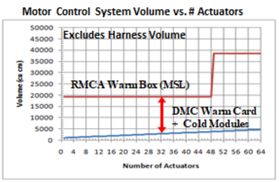
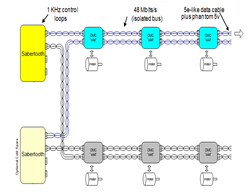



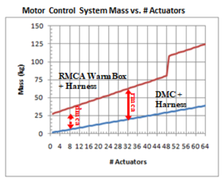

**Figure:** Sabertooth Integrated Processor card

## *Sabertooth Motor Control Layer*

- Distributed Motor Control Architecture
- Design inheritance from M2020 and Mars Helicopter
- All motors connect via a single CAT5 cable
- Improvement in performance while reducing overhead
  - Reduce SWaP
  - Reduce Cable complexity
- HW and SW loop control

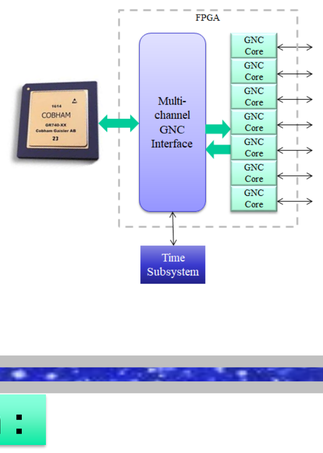


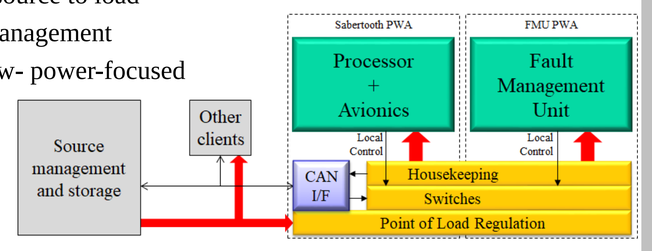

## *Sabertooth GNC Layer*

- Integrated programmable GNC interfaces
  - Provides interface, data strobes/enables/valids
  - Programmable GNC devices
  - Integrated timestamping
- Increase variety and combinations of GNC devi
- No native 1553 support, use alternatives
  - Spacewire,
  - LVDS / 422




## *Sabertooth Power Layer*

- Sabertooth supports a distributed power architecture (DPA) Which is a key element in the significant reduction in power
  - Increased efficiency from source to load
  - Enable fine-grain power management
  - Complemented with the low- power-focused architecture and Sabertooth design
  - GaN devices
  - Supported by efficient flight parts at the load




## PI/Task Mgr. Contact Information :

William Whitaker, Manager,
Advanced Computer Systems and Technologies Group (349C)

William Whitaker@jpl.nasa.gov Tel: (818) 354-7112

## Publications

*Sabertooth: Integrated Avionics for Small Spacecraft Missions*, SCC2019
*An innovative solution for Fault Detection in Small Spacecraft Avionics*, NTR
*Avionics Event Timer Module*, NTR
*Approach for plug and play IP and software auto-detection*, NTR

## Benefits to NASA and JPL:

Our development of a high performance, low mass avionics platform will provide small spacecraft missions with flagship processing and science data throughput at significantly lower power, mass, and cost. This avionics platform will enable NASA/JPL small spacecraft missions to outer planets, Mars, inner planets, and asteroids. Further this avionics platform will enhance the capabilities of small spacecraft Earth science and astrophysics missions.

National Aeronautics and Space Administration
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

www.nasa.gov



RPC-242