

Rapidly Reconfigurable Design, Analysis and Verification Capability for Next Generation Terminal Descent Sensors Principal Investigator: Karthik Srinivasan (334A) Ninoslav Majurec (334C), Razi Ahmed (334C), Michael Tope (334A), Peter Mao (334C) **Program: Topic Area**

Project Objective:

The objective of this work to accomplish two distinct but overlapping tasks,

- To develop generalized landing radar design and performance evaluation tools
- Develop an agile hardware platform capable of testing and demonstrating novel techniques for use in future landing radar missions.

The simulation software leverages MSL legacy tools, evaluating the validity of approximations and expanding their capability to include a variety of EDL/DDL scenarios. Additionally, the proposed effort will include building a reconfigurable hardware platform capable of testing radar designs at different frequencies, including (but not limited to) Ka/W-band that hold potential for reducing the size and power requirements of descent sensors. This hardware platform will be used to test novel approaches that address these challenges such as a hybrid CW/pulsed configuration, AMCW, FMCW and orthogonal waveforms.

Performance Simulator Tool

The varied radar architectures under consideration for landing radars necessitate a simulation architecture that doesn't make the usual assumptions inherent in typical radar raw data simulators.

- The simulator adopts a time-domain point scattering approach (figure 1).
- The scene (figure 2) is divided into individual point targets, each scattering the transmitted waveform (figure 3) back to the receiver weighted by the antenna patterns and radar backscatter (figure 4).
- A simulation step is broken up into programmable update interval



Agile Hardware Test-Bed

The hardware platform was designed for performance verification of the simulator, algorithms and waveforms. The platform is designed to be operated at W-band (figures 5, 6), though additional frequencies can be added on at a later time.

- Built around a 4-channel commercial Software Defined Radio (SDR) for flexibility
- RF Front-End operates at W-band (94GHz)
 - Upconverter translates a 1.335GHz SDR output to 94GHz
- Downconverter translates the received 94GHz signal down to 1.335GHz for the SDR
- Back-end implemented using a combination of FPGA blocks and software, providing the ability to test various waveform and processing techniques
- Target ranging (figure 7) is done via arbitrary waveform pulse compression and autocorrelation peak detection.
- A doppler measurement algorithm based on time domain zero crossings is implemented in the FPGA to measure real time target velocity (figure 7).

ZC doppler





Figure 6: Test Bed Block Diagram



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Benefits to NASA and JPL (or significance of results):

Future robotic lander missions require compact, lightweight Guidance, Navigation and Control (GN&C) sensors. With robotic exploration missions to the Moon, Mars, Europa, Enceladus and Ceres (among others) on the near-to-midterm horizon, there is a need for next generation GN&C sensors that are smaller and lighter than previous sensors. The challenge of designing such a landing sensor is twofold, one is to have well vetted software tools that allow us to explore the design space for a particular mission scenario and analyze performance of relevant radar architectures. The second challenge is to reduce mass and power requirements of a landing radar without compromising reliability and performance. New design approaches that address these challenges need to be tested and demonstrated in realistic scenarios to further JPL's capabilities. The closed-loop design, analysis and verification capability developed in this R&TD effort can be used to design and evaluate the next generation of landing radars for a variety of EDL/DDL scenarios. This effort will deliver a rapid analysis and prototyping capability that will allow the Lab to evaluate various landing sensor configurations, and quickly respond to new opportunities as they arise.

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