

Superlattice-doped, 3D-stacked Hybrid CMOS Detectors

Principal Investigator: Michael E. Hoenk (389)
April D. Jewell (389); Quinn Looker and Marcos Sanchez (Sandia National Laboratories)
Program: Innovative Spontaneous Concepts

Project Objective:

JPL's Advanced Detectors program is collaborating with Sandia's Ultrafast X-ray Imager (UXI) program to develop detectors with unique capabilities for high sensitivity and fast response in extreme radiation environments. Sandia has developed the world's fastest multi-frame digital X-ray imaging detectors capable of time-gated, burst mode imaging. JPL's nanoscale surface passivation process, superlattice doping, hardens these detectors against radiation-induced surface damage, enabling high quantum efficiency and stable response in pulsed-mode detection of high intensity X-rays and low energy electrons. In the final phase of this program, we will develop radiation-hard, time-gated imaging detectors with 1 nm temporal resolution and nearly 100% internal quantum efficiency.

FY18/19 Results:

JPL and Sandia successfully completed a major milestone in our collaboration by fabricating and characterizing n-type superlattice-doped, backside-illuminated photodiode arrays fabricated using advanced 3D chip stacking technologies.

Significant accomplishments completed this year include:

- 1) Demonstrated that JPL's nanoscale surface passivation processes are directly applicable to backside-illuminated, 3D-stacked hybrid CMOS detectors fabricated with copper direct bond interconnect technology (Figures 1 and 2).
- 2) Measured sensitivity of n-type superlattice-doped devices to low-energy electrons near the theoretical limit (Figure 3).

The data presented show that superlattice-doped, 3D-stacked Sandia detectors perform near the theoretical limit for shallow-penetrating radiation (i.e., low energy particles and high energy photon from UV to soft X-rays). We have demonstrated that JPL's nanoscale surface passivation technology, superlattice doping, is compatible with 3D-integration technology that is emerging at the forefront of silicon imaging array production.

Benefits to NASA and JPL (or significance of results):

The work completed under this task has demonstrated that JPL's superlattice doping is compatible with 3D chip stacking technology (Figure 2), which is a core technology for the future of high performance silicon detectors and a crucial technology for future NASA missions. Superlattice-doped detectors have already been baselined for NASA flagship mission concepts LUVOR and HabEx. These results demonstrate that superlattice-doped detectors also offer significant advantages to Lynx, which is another NASA flagship mission proposed for an X-ray survey of the sky. As of today, none of the candidate detectors for Lynx can meet the QE and stability performance that has already been demonstrated with superlattice-doped detectors. Superlattice doping creates a radiation-hard surface passivation layer that eliminates detector instabilities, including hysteresis and persistence; these improvements are essential for achieving precision photometry in scientific imaging and spectroscopy instruments. JPL's superlattice-doping technology can be adapted to any silicon detector and has already been demonstrated on a wide variety of scientific and commercial CCD and CMOS imaging detectors, PIN diode arrays, EMCCDs, and avalanche photodiodes, and will play an essential role in high performance 3D-stacked detectors such as the recently developed photon counting, 3D-stacked Quanta Imaging Sensor (QIS).

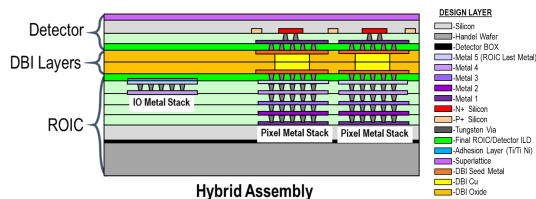


Figure 1. A schematic cross-section of a superlattice-doped, back-illuminated, 3D-integrated device. Sandia's custom ROIC is hybridized with their photodiode devices via copper Direct Bond Interconnect (Cu DBI). The photodiode wafer is back-thinned to expose the photosensitive epitaxial layer and then superlattice-doped at JPL.

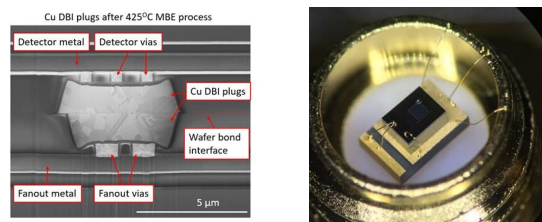


Figure 2. (left) An SEM cross-section of the 3D-integrated device following superlattice doping. Note that the copper interconnects (Cu DBI plugs) and through-silicon vias show no signs of degradation or void formation even after exposure to the high temperature (425 °C) required for the superlattice-doping process. (right) Photograph of a packaged device.

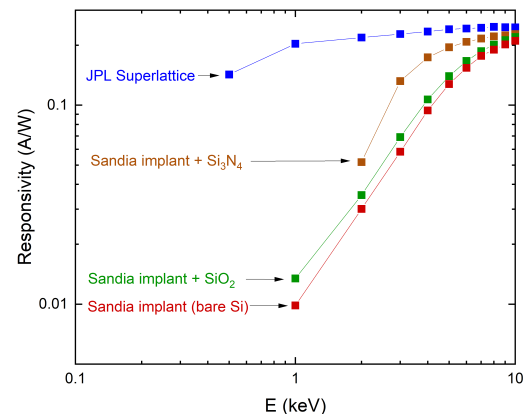


Figure 3. Electron responsivity measurements showing near-ideal performance of superlattice-doped detectors in comparison with conventional ion-implanted devices.

Publications:

Jewell, et al., "Toward Ultrafast, Ultraprecise Imaging Arrays" in preparation.

PI/Task Mgr. Contact Information:

Michael.E.Hoenk@jpl.nasa.gov
Ph. 818-354-1881