Enabling III-V Single Crystalline Growth on Amorphous Substrates for Back-End Integration of Photodetectors on CMOS

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Project Objective:

To establish a growth technology that will enable the integration of III-V IR detector and transistor materials directly on Si ROICs via *back-end processing*. This will enable (i) in-pixel amplification, and (ii) monolithic integration of III-V IR detectors on Si ROICs.

Standard IR detectors use a Si ROIC and III-V detector layers that are interfaced through bump bonding/wafer bonding techniques. This causes significant yield challenges and increases noise. Direct growth of single crystalline III-V templates on the back-end would enable us to utilize metal organic chemical vapor deposition (MOCVD) to then grow high quality detector layers directly on the Si ROIC.

FY18/19 Results:

In FY18-FY19, the team has successfully demonstrated multiple achievements which are critical towards achieving the overall goal of the SURP. These achievements have spanned the areas of material growth, material characterization, device fabrication and measurement, and process development. Specifically, we have achieved the following results:

1. Ultra-low temperature growth of InP and InAs crystalline pixels at temperatures below 400 °C (Fig. 1).
2. Electronic and optoelectronic property interrogation of TF-VLS III-V's demonstrating high quality materials grown via the TF-VLS method. (Fig 2)
3. MOCVD growth of InP and InGaAs on TF-VLS crystals showing highly selective growth of III-V materials on the TF-VLS grown InP. (Fig. 3)
4. Fabrication and characteristics of low-temperature photosensitive FETs. (Fig. 4)
5. Fabrication of low-temperature amplifier FETs. (Fig. 5)
6. Process development for post growth smoothing of surfaces using atomic layer etching showing dramatic improvements in surface smoothness. (Fig. 6)
7. Active pixel circuitry design and simulation (Fig. 7)

Benefits to NASA and JPL (or significance of results):

Today, shortwave infrared (SWIR) focal plane arrays (FPAs) are manufactured using a complex process with many steps that are performed at the individual die level. A complete process flow typically takes several months, has low yield, and therefore individual science grade FPAs frequently cost tens of thousands of dollars. This complex process is required because obtaining high-quality, small-bandgap semiconductors requires that they be deposited at high temperatures on an expensive crystalline substrate. The thermal budget of CMOS wafers is too low for typical crystal growth, and while the wafers are crystalline, the surface of CMOS wafers is composed of metals and/or amorphous insulators. This thermal limit and the inherently non-epitaxial CMOS substrate has, to date, made it impossible to produce scientific grade semiconductor detectors of sufficient quality to achieve state-of-the art NASA mission goals directly on Read-out Integrated Circuits (ROICs) at wafer scale. It is noted that the significant cost and lead-time of science grade SWIR sensors limit the design of even world-class IR instruments such as Euclid. For example, to overcome these limits, Euclid adopted a dual focal plane with small pixel CCDs to measure galaxy shapes and large pixel IR arrays to measure photometry. However, a new technology, thin film-vapor liquid solid growth (TF-VLS) has shown the ability to produce high quality III-V material for phototransistor and solar cell fabrication, even when grown on silicon dioxide and molybdenum substrates. This SURP effort took the first steps to leverage and apply this excellent device material towards IR detectors.

Results:

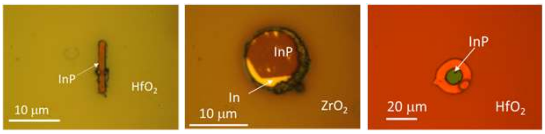

Fig 1; Ultra-low temperature growth of InP and InAs crystalline substrate layers

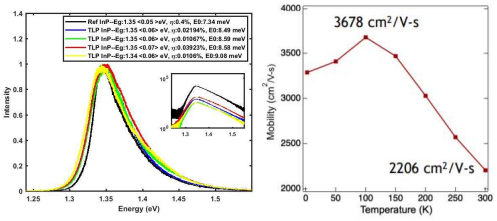

Fig 2: Electronic and optoelectronic property interrogation of TF-VLS III-V

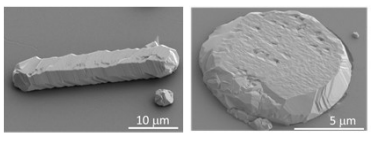

Fig 3: MOCVD growth of InP and InGaAs on TF-VLS crystals

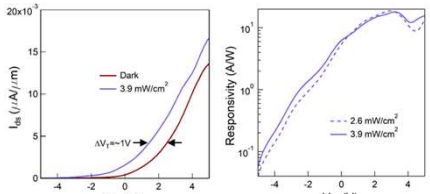

Fig. 4: Fabrication and characterization of low-temperature photosensitive FETs

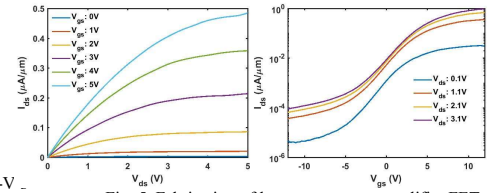

Fig. 5: Fabrication of low-temperature amplifier FETs

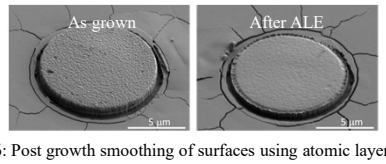

Fig. 6: Post growth smoothing of surfaces using atomic layer etching

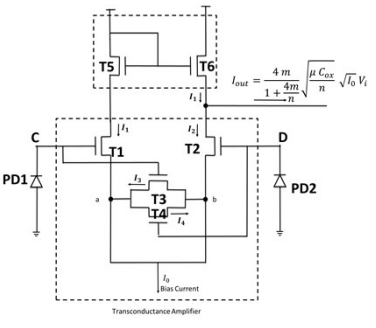

Fig. 7: In pixel amplifier design

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Publications:

1. D. Sarkar et. al Device Research Conference Paper
2. D. Sarkar et. al Electronic Materials Conference Paper

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