Virtual Research Presentation Conference

Small Spacecraft Avionics Subsystem for Planetary Science Missions

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Tutorial Introduction

Abstract

The overall objective of the task is to develop the small spacecraft avionics system and achieve a maturity of TRL 5. The objective in FY20 was to develop the bulk of software and firmware and perform the ambient testing in preparation for relevant environment testing in FY21.

- There are four main objectives to accomplish this goal.
    1. Complete the PCI and the AMBA interface from the Sabertooth FPGA to the processor
    2. Complete the Fault Management Unit health collection logic
    3. Demonstrate application of flight software drivers for processor interfaces
    4. Complete the Sabertooth NAND controller FPGA IP and the file system software/driver and demonstrate in the lab

Dual String Sabertooth Avionics

Problem Description

Small spacecraft planetary space science missions require development of subsystems with high performance, low mass and power, long life capabilities at a much lower cost. The state-of-practice large spacecraft subsystems are not suitable for small spacecraft applications as they are heavy, power hungry and costly. The state-of-practice CubeSat subsystems are also not suitable for future small spacecraft planetary science missions due to their limited performance capabilities, limited reliability and life.

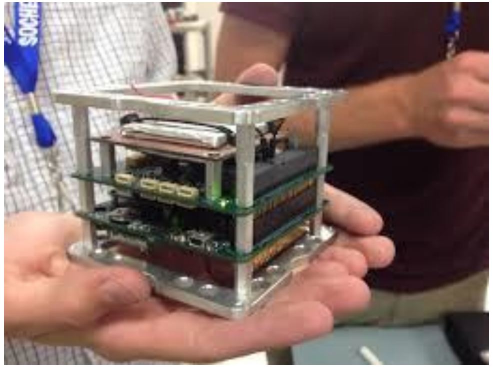
Large Spacecraft Avionics

The Good

- long life and
- high reliability
- High capabilities

The Bad

- power hungry,
- Heavy
- costly.



Cubesats

The Good

- low power
- Low mass
- Low cost

The Bad

- poor performance
- Poor life reliability
- Poor radiation

Comparison to the State of the Art

The Sabertooth Small Spacecraft Avionics offers several advantages compared to the state of practice C&DH systems of large planetary spacecraft and CubeSat. Some of the specific benefits of the integrated avionics platform compared to RAD750 based large spacecraft C&DH systems are: a) 8X CPU performance, b) 20X throughput capability, C) 5X lower mass, and d) 6X lower power.

As shown in the table below, our goal is to improve upon state of the art avionics:

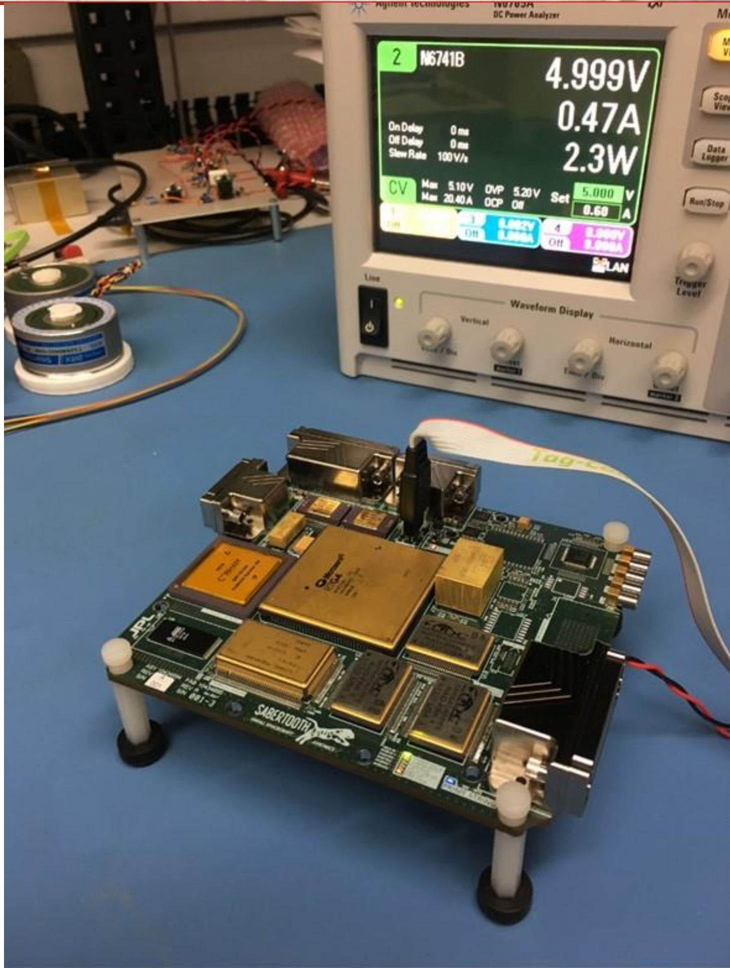
quantitative capability goals	Goals for this proposal	CubeSat SoA	Industry SoA	JPL SoA
CPU: Cores	Quad Core	Dual Core	Single Core	Single Core
CPU: Performance	1200 MIPS	270 MIPS	266 MIPS	266 MIPS
Power	<10 W	4W	20.2 W	58 W
Mass	4 kg	55 g	20 Kg	50 kg
Size	17cm x 17cm	1 U (10cmx9.4cm)	3U	3U / 6U
Radiation: CPU	300 Krad	300 Krad	1 Mrad	1 Mrad
Radiation: Other board parts	30 Krad	30 Krad	30 Krad	30 Krad
A/B string support	Dual	Single	Dual	Dual
SpaceWire Interface support	Yes	Yes	Yes	-
UART Interface support	Yes	Yes	Yes	Yes
I2C Interface support	Yes	Yes	Yes	-
SPI Interface support	Yes	Yes	-	-
Integrated DMC Motor Control	Yes			
Integrated Radio/Telecom	Yes	-	-	-
Integrated GNC	Yes	-	-	-
Distributed POL Converters	Yes	-	-	-

Relevance to NASA and JPL

The Sabertooth avionics subsystem will provide small spacecraft missions with flagship processing and science data throughput at significantly lower power, mass, and cost.

Further, this new avionics subsystem will enable the use of small probes with reliability in larger missions (e.g. Discovery, New Frontiers, and Flagship missions), enabling new science discoveries.

This avionics platform will enable NASA/JPL to small spacecraft missions to outer planets, icy moons, inner planets, and asteroids.



Sabertooth Processor

Methodology

The goal of this strategic initiative is to mature the platform to TRL5 and enable proposers to propose the Sabertooth avionics after FY21. The approach for this year at a high level was to develop core software and hardware in preparation for verification of the Sabertooth as an integrated avionics platform in a relevant environment.

As we are validating an avionics subsystem at TRL5 as opposed to a flight computer, this year involved a fair amount of low-level development of core avionics functions, For hardware we have adopted the use of industry IP cores whenever possible. For Flight Software we use the F-prime framework. We are validating the integration of these functions, exercising test procedures, and generating expected results. These will be a applied in the run for record relevenat environment testing in FY21.

Results

For FY20 the following goals were stated in our proposal:

1. Complete the PCI and the AMBA interface from the Sabertooth FPGA to the processor
2. Complete the Fault Management Unit health collection logic
3. Demonstrate application of flight software drivers for processor interfaces
4. Complete the Sabertooth NAND controller FPGA IP and the file system software/driver and demonstrate in the lab

This year, we achieved all of our goals for development and delivery of Software and hardware for the platform except for #4. We consider this not complete despite having the FPGA IP and software drivers in-hand . A file system requires a fair amount of lab testing between the software, firmware, and hardware developers to consider being done and that was not achievable given the challenges presented by COVID 19. This work has been scheduled to go into FY21 and ideally would occur once we return to the lab and can have the majority of the team simultaneously in the lab.

The remainder of the goals where successfully achieved

Significance of Results

The goal for FY20 was to develop the low-level functionality of the Sabertooth and test in a laboratory environment in preparation for repeating these tests in a relevant environment in FY21. The success of the work performed over the year puts us in position to achieve this goal. Specific results include

- Completing this effort provides flight-ready FPGA cores, flight software, test-benches and documentation to every future Sabertooth mission as a zero RE cost item, This enables future Sabertooth missions to procure industry-available elements and manage costs and schedule.
- We successfully implemented and tested a significant improvement to fault detection and management, as presented in NTR 50956 (An innovative solution for Fault Detection in Small Spacecraft Avionics) .
- The software managers and drivers completed represent low-level software unique to the Sabertooth platform and the GR740 and is the software that will be reusable by every future Sabertooth mission as a zero RE cost item.
- Our Success ar leveraging industry IP for all of the components between the processor and the file system memory is a significant step in reducing the cost to future missions.
- We have built up a fair amount of functionality over the past year and are maintaining power at around 5W, which is under our target goal.

Next Steps

The next steps for the last year of this task include:

- Complete the NAND flash controller
- Complete the ambient testing.
- Identify the relevant environment criteria for the TRL 5 validation, and repeat the ambient test suite in an environmental chamber

Publications and References

1. William Whitaker, “Sabertooth: Integrated Avionics for Small Spacecraft Missions,” *Space Computing Conference*, 2019.