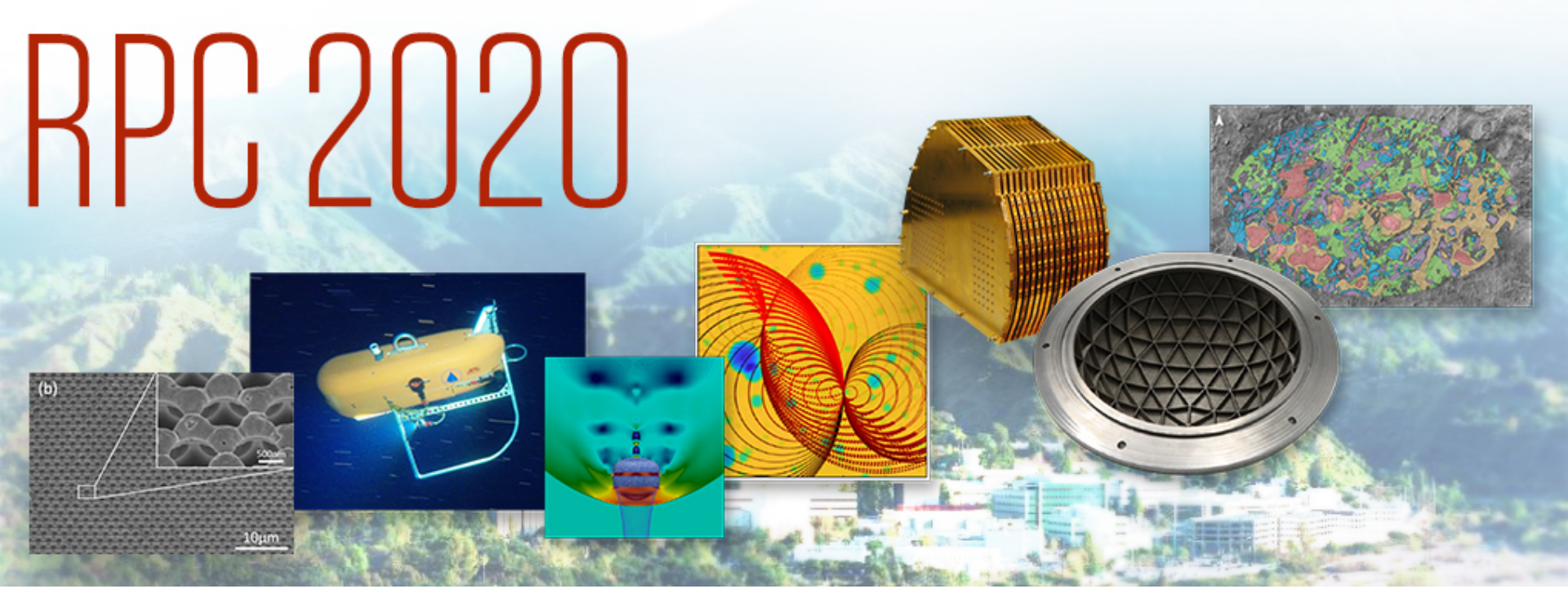
RPC 2020



Virtual Research Presentation Conference

PanFTS – DFPA Electrical/Data Interface, Real-Time Processing and Validation at CLARS

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Program: Strategic Initiative

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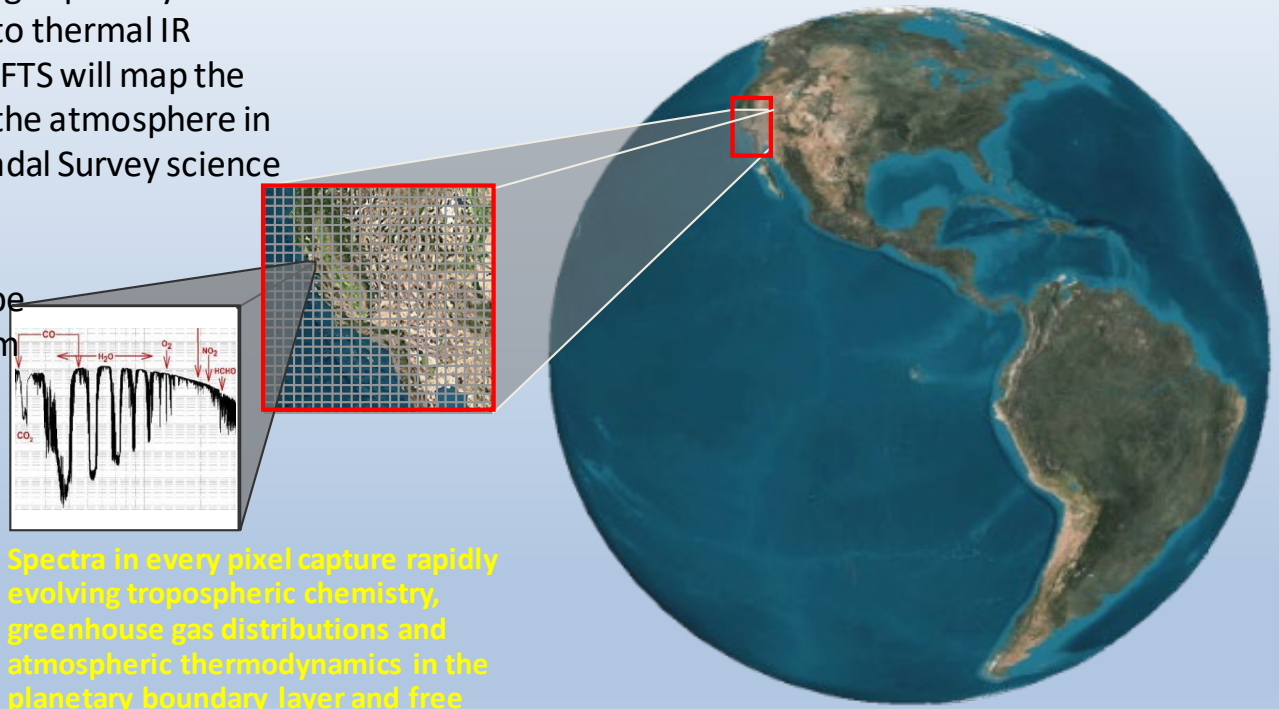
Jet Propulsion Laboratory
California Institute of Technology

Geostationary Imaging Fourier Transform Spectrometer (PanFTS): Hourly Sampling of Trace Gases

- PanFTS is an ultra wide-band Fourier Transform Spectrometer with 2-D imaging capability. Spectral coverage is near-UV to thermal IR
- From geostationary orbit, PanFTS will map the abundances of trace gases in the atmosphere in support of Earth Science Decadal Survey science objectives
- Greenhouse gases, pollutants chlorophyll fluorescence will be measured hourly with ~few km spatial resolution
- PanFTS will be hosted on a geostationary comsat. This approach is being used to accommodate other NASA instruments including TEMPO and GeoCarb.



Spectra in every pixel capture rapidly evolving tropospheric chemistry, greenhouse gas distributions and atmospheric thermodynamics in the planetary boundary layer and free troposphere

From geostationary orbit PanFTS can map all of North and South America hourly with high resolution measurements (temporal, spatial, and spectral) that capture rapidly evolving tropospheric concentrations with planetary boundary layer sensitivity

Goal

- The goal of this task is to advance the maturity of two key components of the PanFTS instrument to improve its readiness for a NASA Explorer-class or Earth Ventures opportunity

Task Objectives

1. Design, build and test an electrical interface between a digital focal plane array (DFPA) provided by MIT-Lincoln Laboratory and the PanFTS data acquisition system
   - Key design requirements include a path-to-flight processor (Xilinx Kintex Ultrascale FPGA)
   - Capability to process 640x480 pixel images at 1000 frames s^{-1} (~ 5 Gbps)

2. Design, build and test an onboard processing system to convert raw data (interferograms) into radiance spectra
   - Onboard processing will reduce the downlink data rate by about 20X.
   - The goal is to minimize the operating cost to lease transponders from the owner/operator of the host comsat

Methodology and Results (1/2)

This fiscal year (year 2 of 3 for this task), a number of important milestones were achieved:

Interface Hardware

1. Completed the low-level design, schematic and layout of the DFPA interface
   - The interface preforms readout and pre-processing including flat-field calibration, pixel binning and windowing
   - Pre-processed data is transmitted off-board through either a Gigabit Ethernet port or a SFP+ 10G Ethernet port
   - The board includes an interface to the analog-to-digital converters that digitize the metrology laser interference fringes, and synchronization of the fringes with FPA frame capture
2. Acquired parts, sent for fabrication to Sierra Circuits
3. Performed initial power subsystem checkouts including power sequencing checks and min/max load checks for power rails
4. Interfaced to an unhybridized DROIC (digital readout integrated circuit) from MIT-Lincoln Labs for fit checks and read/write tests prior to connection to the actual DFPA

Methodology and Results (2/2)

FPGA Development

- Emulation of the Lincoln Labs DROIC data stream
- Frame buffer realignment of data based on enabled DROIC taps
- Flat field calibration support through gain and offset of each individual pixel
- Pixel binning to allow 2x2 pixel fields to be combined into a single pixel
- Pixel masking, where specific pixels are removed from the frame, allowing for compression
- Gigabit Ethernet and UART interface using a python command line application on a PC
- Configuration of DROIC parameters
- TCPdump support for incoming ethernet data
- Troubleshooting features

As-built DROIC Interface

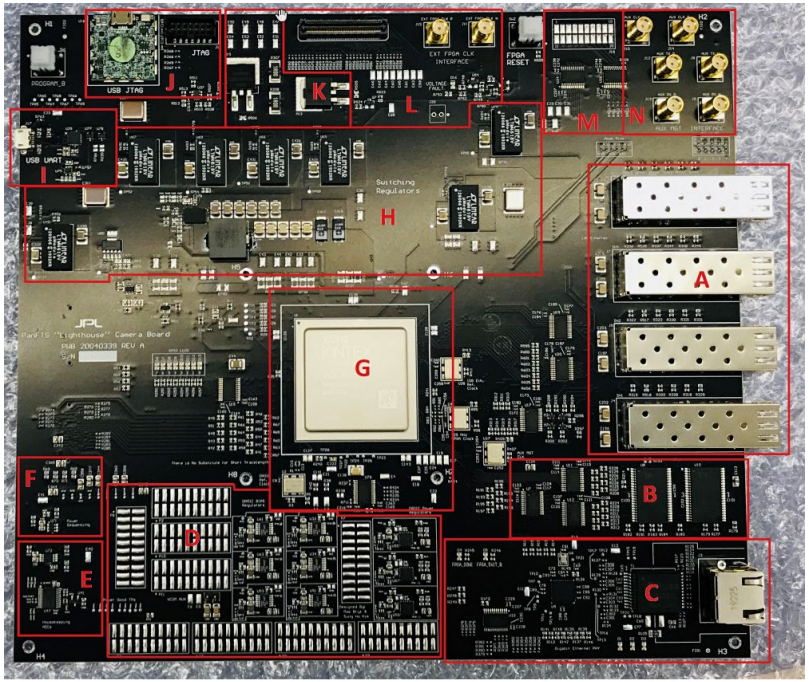


Figure 1. . Photo of the Lighthouse interface board. A – 4x 10G Ethernet Ports, B – Non-volatile memory (MRAM), C – RJ45 Gigabit Ethernet Subsystem, D – DROIC Biases Subsystem, E – Housekeeping ADCs, F – Power Sequencing Subsystem, G – KCU060 Xilinx Kintex Ultrascale FPGA, H – Switching regulators power subsystem , I – USB UART, J – JTAG interfaces, K – Power interface and soft-start circuitry, L – Auxiliary connections and external FPGA clock interface , M – Metrology Laser ADC interface , N – Auxiliary connections

Assessment and Future Plans

Assessment

- The design, fabrication and preliminary testing of the DROIC interface has been completed
- FPGA code to control the acquisition, timing and processing of FPGA imaging data has been completed.
- Additional testing of the hardware and FPGA code are underway.
- When completed, JPL will have a fully functional interface to the MIT-Lincoln Lab DROIC which will be configurable for present and future needs
- The interface has the capability to synchronize the interferometer image data with metrology laser fringes which is required to transform the interferograms into spectra.

Plans for FY21

- Integrate the DFPA, interface, data system into the PanFTS testbed interferometer in B306 and acquire atmospheric spectra using the lab's heliostat.
- Acquire additional atmospheric spectra from JPL's CLARS remote sensing lab on Mt. Wilson

Publications and References