# RPC 2020


## Advanced 25 nm Gate Length Low Noise Amplifier (LNA) in Indium Phosphide (InP) High Electron Mobility Transistor (HEMT) Monolithic Microwave Integrated Circuit (MMIC) Technology for Broadband X- Through Ka- Band Receivers

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**Program: Spontaneous Concept**

Assigned Presentation RPC-288

# Tutorial Introduction

**Abstract**

JPL NASA is responsible for solar system exploration and deep space navigation

This requires the development of a data base of reference objects in space

Mappings of distant objects like quasars have been primarily at S- band (2.3 GHz) and X- band (8.4 GHz)

New reference frame mapping developments are targeting dual X- and Ka- band (32 GHz)

The goal of this project is to develop the best broadband low noise amplifiers (LNAs) to enable the lowest noise receiver system to support the next generation instrument for reference frame observations for navigation at both X- and Ka- band simultaneously

# Problem Description

a) S-band observations have increasing radio frequency interference (RFI) and is being phase out. There is a need to advance and go to higher frequency observations such as Ka-band where higher resolution observations can be made to define finer structure reference objects and also operate where there is less RFI

b) Commercially there are very good narrower band LNAs at X- band and at Ka-band however there has been no commercially or readily available LNAs that cover both bands simultaneously. A single broadband system with good performance would be less costly to build and maintain than a two receiver system covering each band separately. The pursuit of the best performance LNA to enable a broadband system is the goal of this effort.

c) Only recently did we developed a record low noise X- to Ka- band LNA using Northrop Grumman Corporation's 35 nm gate length high electron mobility monolithic microwave integrated circuit process [1]

d) The purpose of this spontaneous effort is to leverage an opportunity that materialized to utilize NGC's most advanced 25 nm gate length process [2] to develop new and improved broadband LNAs

e) These new high performance LNAs we develop will allow JPL to lead the development of the hardware and its application to improve reference frames into the future

# Methodology

a) An approximate expression of minimum noise temperature (Tmin) of a HEMT is given by,

$$T_{min} = (F/F_{max})*(T_a*T_d)^{(1/2)},$$

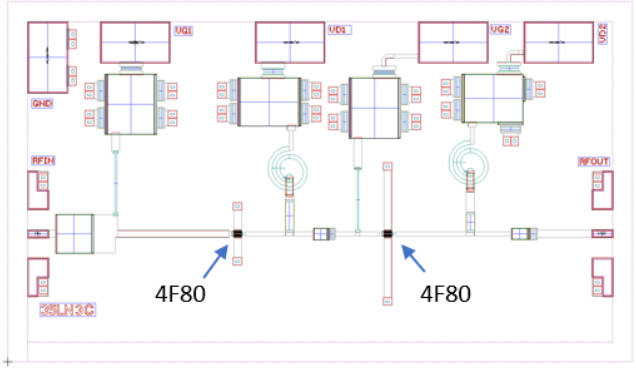
where F is the frequency, Fmax the power gain cutoff frequency, Ta the ambient temperature and Td the effective drain temperature [3]. It can be seen that higher Fmax supports lower noise performance, however scaling gate length shorter has the tendency of increasing a transistor's drain temperature also and thus has an opposite effect of increasing noise. Below about 50 GHz with the available data of existing LNAs it is less conclusive what the optimal gate length is for the lowest achievable noise LNA, that is what term in the Tmin expression, Fmax or Ta is more dominant. It is possible that the 25 nm process with Fmax of 1.5 THz could provide for a LNA with better performance than the 35 nm process. This effort explores this possibility.

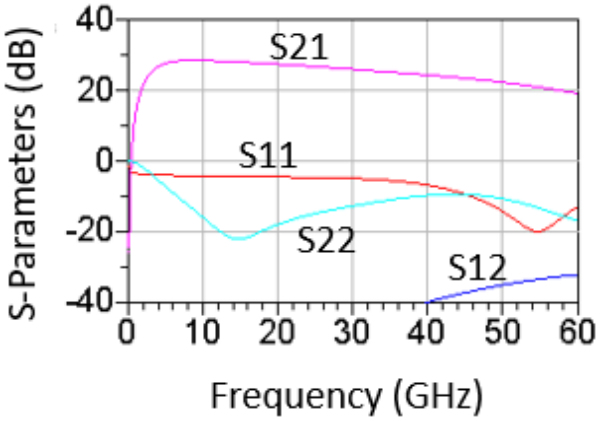
b) To design our LNAs we examined the gain, noise and stability circles of the HEMT to determine the target input impedance match for low noise while providing desired gain and stability of the transistor. The output of the transistors were conjugately matched and impedance transformed to the next transistor stage's target input impedance. The input and output impedances of the LNAs were all transformed to 50 ohm coplanar waveguide ground-signal-ground probe pads for on-wafer probing and packaging. Microstrip was used for the wiring environment; different microstrip impedance lines, capacitors, inductors, and resistors were used for impedance transformers and the bias networks. The number of transistor stages used in a LNA was chosen to provide the overall desired LNA gain, which we targeted at least 20 dB.

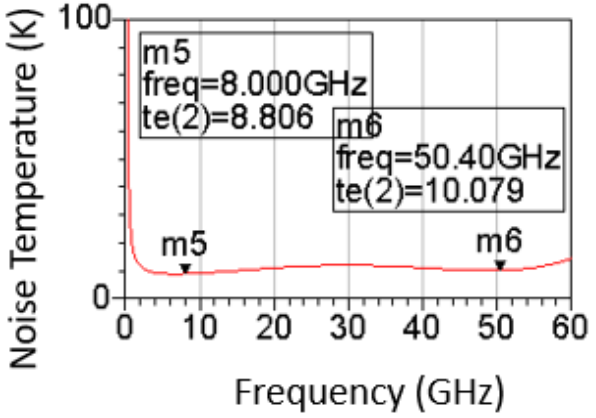
# Results

a) The performance at 20 K ambient of LNA design 35LN3C (one of the three) is shown below,

35LN3C Layout




b) The simulated bandwidth of 35LN3C and its noise at the higher portion of the frequency band is better than the simulated performance of our record broadband and low noise 35 nm LNA [1]

c) Due to possible inconsistencies between models and fabrication, post fabrication measurements are needed to ve
35LN3C improves on the state-of-the-art

# References

[1] Andy Fung, Lorene Samoska, James Bowen, Steven Montanez, Jacob Kooi, Melissa Soriano, Christopher Jacobs, Raju Manthena, Daniel Hoppe, Ahmed Akgiray, Richard Lai, Xiaobing Mei, Michael Barsky, “X- to Ka- Band Cryogenic LNA Module for Very Long Baseline Interferometry,” Proc. IEEE-MTT Int. Microwave Symp., 2020.

[2] Xiaobing Mei, Wayne Yoshida, Mike Lange, Jane Lee, Joe Zhou, Po-Hsin Liu, Kevin Leong, Alex Zamora, Jose Padilla, Stephen Sarkozy, Richard Lai, William R. Deal, “First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process,” IEEE Electron Device Letters, Vol. 36, No. 4, April 2015.

[3] Marian W. Pospieszalski, “On the limits of noise performance of field effect transistors,” Proc. IEEE-MTT Int. Microwave Symp., 2017.