Virtual Research Presentation Conference

Alternative Methods for Acceleration of Wavefront Control Computation for Large Space Telescopes

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Program: SURP

Assigned Presentation #SP20011

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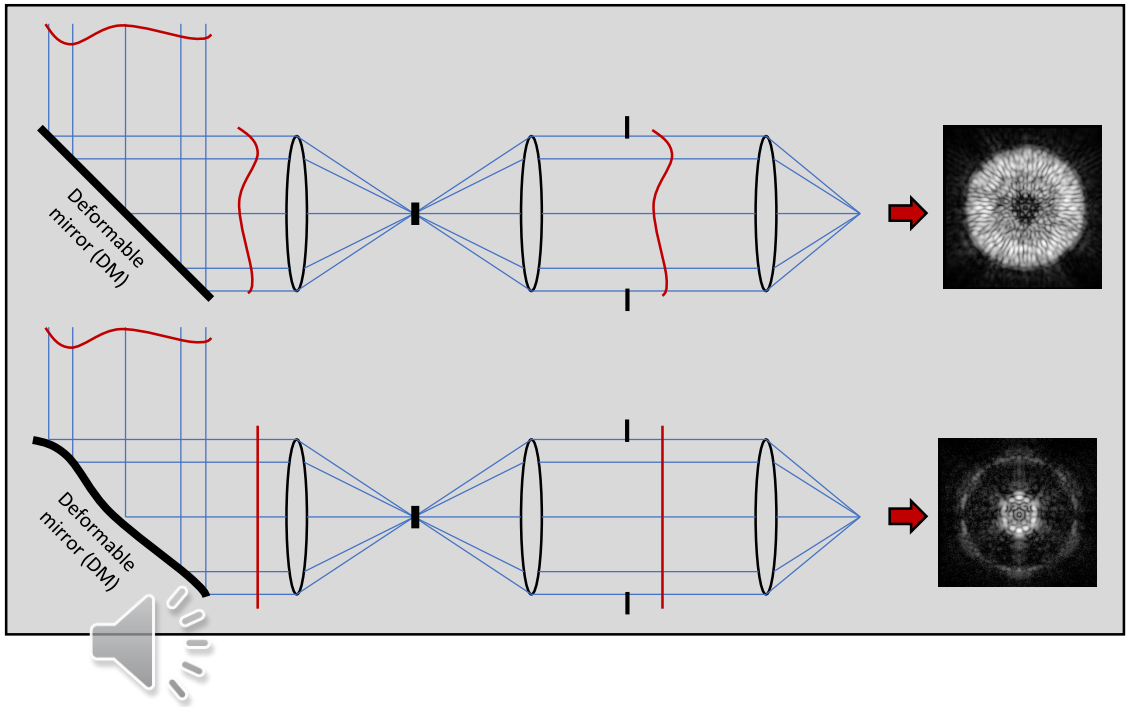
Tutorial Introduction

Coronagraphs are optical instruments designed to look for very faint objects right next to brighter ones, such as exoplanets next to their host stars

- They use a series of optical masks to selectively filter out the starlight
- Their performance will be degraded by misalignments or imperfections in optical surfaces

Wavefront sensing and control (WFSC) systems measure the effect of those imperfections and move deformable mirrors (DMs) to cancel those effects out.

Without WFSC, most coronagraphs in real instrument systems would be unable to see exoplanets.



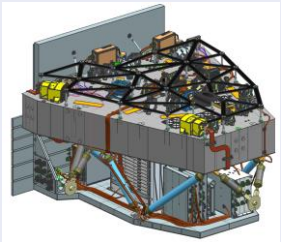
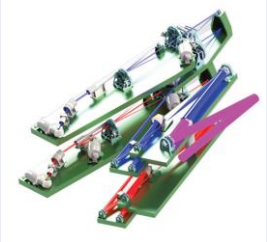
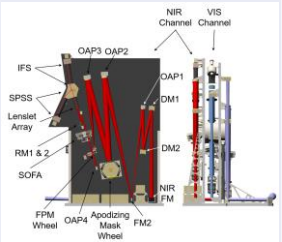
Problem Description

Context: HabEx and LUVOIR are two of the four candidate large missions proposed to the 2020 Decadal Survey in Astronomy and Astrophysics as follow-ons to JWST

- Both have coronagraphs proposed for imaging exoplanets, with WFSC systems
- Both are baselining on-board computation for WFSC.
- Both are expecting to use larger-format DMs than current state-of-the-art (SOA) instruments

The challenge:

- WFSC computation and storage costs scale steeply with DM size (N^4 - N^6 depending on algorithm choices)
- Suitable rad-hard flight processors do not seem to be on track to scale up at this rate

	Roman Space Telescope (Roman)	Habitable Exoplanet Observer (HabEx)	Large UV-Optical-Infrared Surveyor (LUVOIR)
Instrument	CGI	HCG	ECLIPS
			
Status	In development at JPL (Phase C)	Proposed	Proposed
WFSC computation baseline	Ground-in-the-loop (was on-board rad-hard avionics)	On-board rad-hard avionics	On-board rad-hard avionics
Deformable mirror size (N×N)	2 48x48 DMs	2 64x64 DMs	2 128x128 DMs
Computation/storage cost relative to SOA (N^4 - N^6)	1	3.2 - 5.6×	50.6 - 359.6×

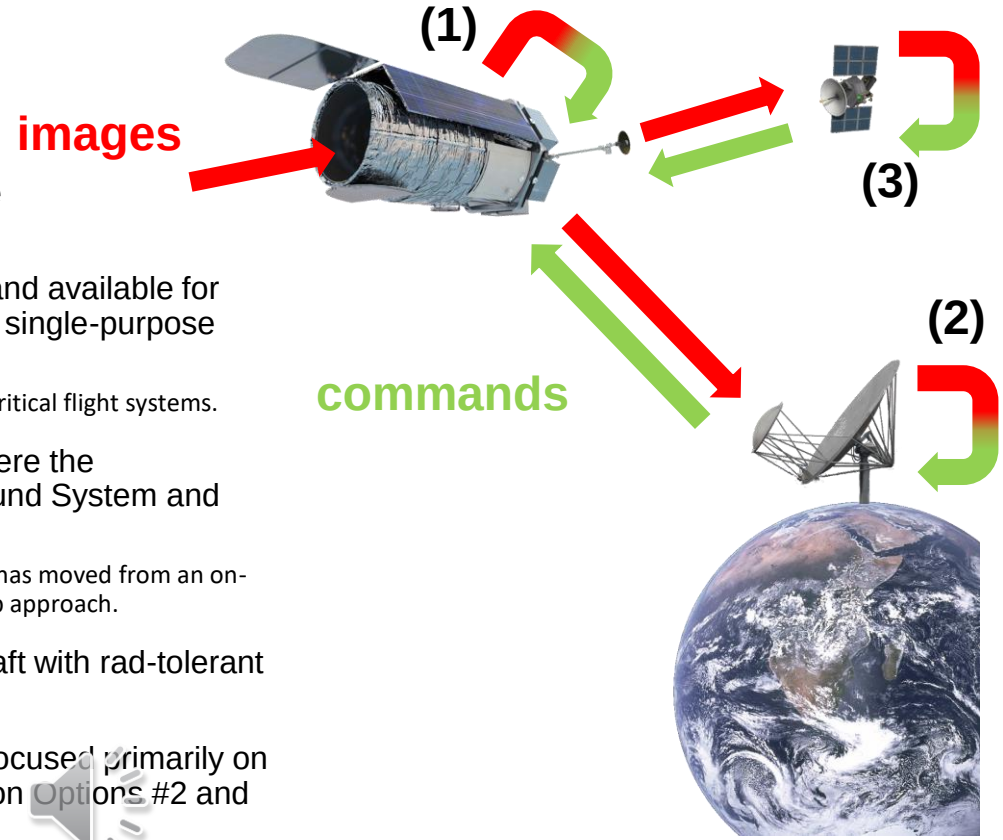
The problem: *If the processing capability of space-qualified hardware does not advance faster than the increase in desired deformable mirror actuator counts, these observatories may have their high-contrast science return limited by processing overheads of wavefront control.*

Methodology

Our proposal: we will do a trade study between a baseline case (on-board rad-hard processing and storage) and three alternatives with the potential to offer higher performance:

1. Evaluate the use of rad-tolerant processors developed and available for commercial applications for use within an instrument for single-purpose WFSC computation.
    - These would be in addition to standard rad-hard processors for critical flight systems.
2. Evaluate the use of ground-in-the-loop computation, where the computationally-intensive parts are done within the Ground System and data is passed back and forth.
    - Note: since the start of this SURP, the CGI instrument on Roman has moved from an on-board rad-hard approach to computation to a ground-in-the-loop approach.
3. Evaluate the use of a dedicated co-flying small spacecraft with rad-tolerant COTS processors for offloading computational needs

This work was planned to span 2 years, with the first year focused primarily on the baseline and Option #1, and the second year primarily on Options #2 and #3.



Results

Year 1 work:

- Identify trade study Musts and Wants to permit comparison of disparate WFSC architectures
- Perform literature and community research to identify key wavefront sensing and control algorithms
- Evaluate computational complexity of each of the key algorithms
- Perform literature and community research to identify the computational capability of key processors that are candidates for future flight projects (both rad-hard and rad-tolerant COTS)
  - Div 51x personnel provided assistance with this
- Build tools to parametrically evaluate performance for different use-cases (e.g. HabEx, LUVOIR) as a function of algorithm and processing architecture

With these tools we can combine the processor and memory capability with the computational complexity of the algorithms for an example case, and look at the time required to reach a nominal benchmark performance level

Processor	Clock Speed (MHz)	Core Architecture	Cores	Core Bits	Dedicated FPU with MAC	External Memory Interface/Controller
BAE RAD5545	466	PowerPC e5500	4	64	Yes, compiler-dependent	DDR3 at 800 MHz
BAE RAD750	200	PowerPC 750	1	32	Yes, compiler-dependent	Parallel SRAM
Vorago VA41620	100	ARM Cortex-M4F	1	32	Yes	Parallel SRAM w/ DMA Controller
SnapDragon 855	2420	ARM Cortex-A76	4/8	64	Yes	LPDDR4X at 2133 MHz
Renesas Cortex-R4F	600	ARM Cortex-R4F	1	32	Yes	Parallel SRAM w/ DMA Controller
TI Cortex-R5F (TMS570)	300	ARM Cortex-R5F	1	32	Yes	Parallel SRAM w/ DMA Controller
ST Stellar R52	400	ARM Cortex-R52	4/6	32	No	Parallel SRAM

			Computation Time (hours)						
			Rad-Hard			Rad-Tolerant COTS			
			BAE RAD5545	BAE RAD750	Vorago VA41620	SnapDragon 855	Renesas Cortex-R4F	TI Cortex-R5F (TMS570)	ST Stellar Cortex-R52
Algorithm	Precomputation	Jacobian precomputation	185.76	497.99	820.22	71.94	181.81	248.80	192.24
		EFC gain precomputation	94.60	253.61	417.71	36.64	92.59	126.70	97.90
	Estimation Step, per iteration	Pairwise probing	0.05	0.14	0.23	0.02	0.05	0.07	0.05
		Self-coherent camera (SCC)	< 0.01	< 0.01	< 0.01	< 0.01	< 0.01	< 0.01	< 0.01
	Control step, per iteration	Electric field conjugation (EFC)	0.22	0.60	0.99	0.09	0.22	0.30	0.23
		EFC (with precomputed gain)	0.01	0.04	0.06	0.01	0.01	0.02	0.01
		Jacobian update with E-M (adaptive)	0.27	0.71	1.17	0.10	0.26	0.36	0.27
	Maintenance	Linear dark field control (LDFC)	0.21	0.57	0.95	0.08	0.21	0.29	0.22
		EFC with extended Kalman filter	0.22	0.60	0.99	0.09	0.22	0.30	0.23

Publications and References

Computational Requirements of Focal Plane Algorithms for High Contrast Imaging in Space Telescopes [in prep for JATIS]