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Virtual Research Presentation Conference

Monolithic High-Performance Infrared Detectors on Silicon Substrates for Integrated Photonics

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Program: (SURP)

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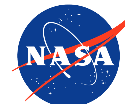

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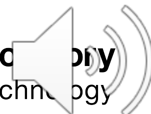
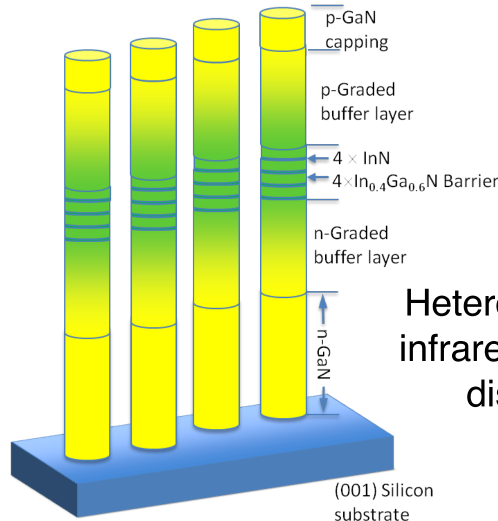


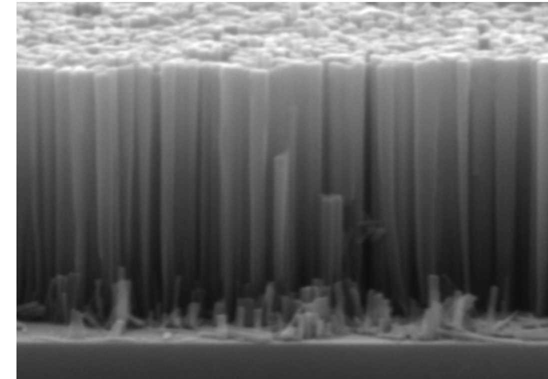
Tutorial Introduction

Abstract

The objective of this proposed work is to investigate and demonstrate III-nitride monolithic nanowire array infrared (IR) detectors on silicon substrates operating at high temperatures. An important fabrication step in the realization of current high performance detector array technologies for IR focal plane arrays is the indium-bump bonding of the detector arrays onto silicon based readout integrated circuits. This costly and sometimes unreliable step is necessary because almost all current IR detection technologies are based on semiconductor heterostructures homoepitaxially grown on non-silicon substrates. But, a silicon based monolithic detector array technology can eliminate this undesirable indium-bump bonding process.



Heterostructure of near-infrared (λ~1700nm) InN disk-in-nanowire



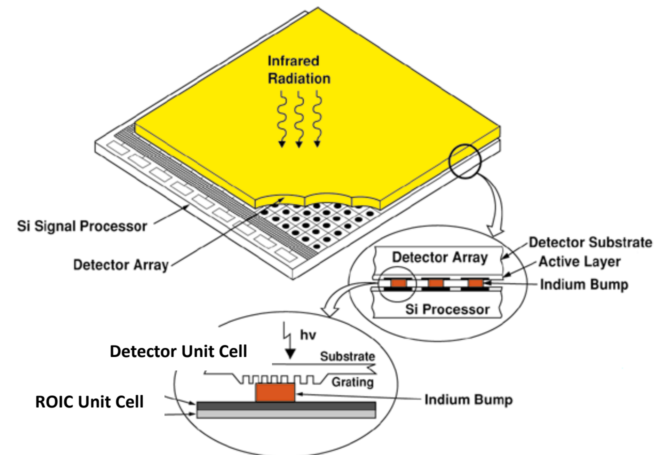
Scanning electron microscope image of N nanowire array epitaxially grown on (001)i

Problem Description

a) An important fabrication step in the realization of current high performance detector array technologies for IR focal plane arrays is the indium-bump bonding of the detector arrays onto silicon based readout integrated circuits. This costly and sometimes unreliable step is necessary because almost all current IR detection technologies are based on semiconductor heterostructures homoepitaxially grown on non-silicon substrates. But, a silicon based monolithic detector array technology can eliminate this undesirable indium-bump bonding process.

b) Current state-of-the-art (SOA) infrared focal plane array (FPA) fabrication technology is based on detector array and read out integration circuit (ROIC) hybridization process via indium bump interconnects. This process is time consuming and expensive, because, it has to be performed at individual die basis. FPA hybridization process is a complicated process and it lowers the yield. In addition, it lowers the pixel-to-pixel uniformity and pixel operability as well.

c) Therefore, a monolithic silicon-based IR detection technology demonstration is relevant to NASA applications. Thus, demonstration of a viable silicon-based detector array technology will be a major breakthrough.



This figure shows the non-silicon detector array hybridization process with a silicon CMOS ROIC via indium bump bonding process

Methodology

The infrared detectors are fabricated with epitaxially grown III-nitride disk-in-nanowire heterostructures on silicon and characterized for eventual application in silicon-based FPAs for low cost high performance IR observational instruments.

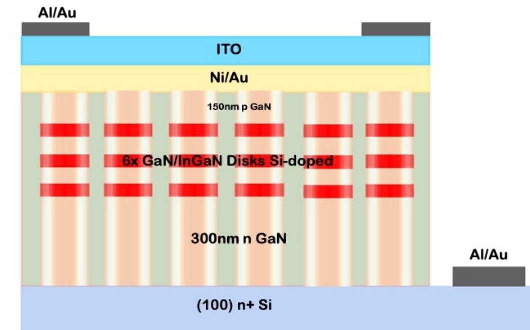
Our approach is,

a) Design InGaN/GaN dot-in-nanowire heterostructure infrared detectors

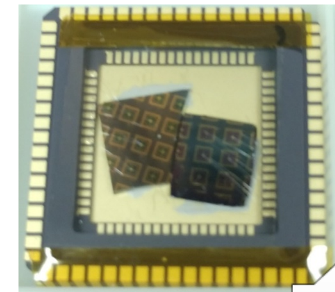
b) Grow n (GaN) – i (InGaN/GaN dot/barrier) – n (GaN) dot-in-nanowire heterostructure arrays on (001) silicon substrates using molecular beam epitaxy [1]

c) The overall fabrication was done in three steps of lithography process, mesa patterning, bottom contact, and top contact. Prior to everything, NW samples were planarized with parylene. ITO was used as the current spreading layer. Ni/Au and Ti/Au were used for P and N contact respectively. All of the samples were seen under scanning electron microscopy to confirm the desired morphology, like NW height, NW diameter, thickness of planner template, smoothness of the top planer surface, etc. The optical behavior was confirmed with steady state photoluminescence spectroscopy. The dot regions are selectively doped n-type for stronger electron intersubband absorption. After growth of the nanowire heterostructure arrays, they are planarized and passivated with parylene. The contact on silicon (bottom) is formed by Al and the top contact is formed on top of the nanowire photoconductive detectors, with ITO.

d) Measure the quantum efficiency and dark current density as a function of device operating temperature



This figure shows the device structure of the $In_{0.34}Ga_{0.66}N/GaN$ disk-in-nanowire arrays detector.



This figure shows the $In_{0.34}Ga_{0.66}N/GaN$ disk-in-nanowire arrays detectors on a 68-pin lead-less chip carrier.

Results

a) Grown and fabricated six InGaN/GaN dot-in-nanowire heterostructure device structures.

b) To summarize, we have grown, fabricated, and tested six device samples. The infrared photoluminescence spectrums clearly show (see Fig. 1) photoluminescence from the $In_{0.34}Ga_{0.66}N$/GaN disk-in-nanowire arrays. As we expected the IV curves show (see Fig. 2) diode like characteristics. Infrared absorption measurements are being carried out to determine the infrared intersubband absorption of $In_{0.34}Ga_{0.66}N$/GaN disk-in-nanowire arrays.

c) However, couldn't complete the full characterization of these devices due to COVID-19 issue. The next step will be the complete the device characterization process.

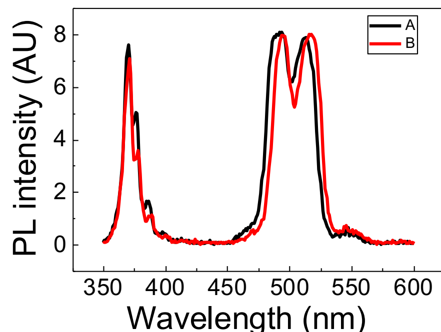


Figure 1. Photoluminescence intensity vs. wavelength of an $In_{0.34}Ga_{0.66}N$/GaN disk-in-nanowire arrays. Curves A and B are two photoluminescence spectrums taken at difference places of the sample.

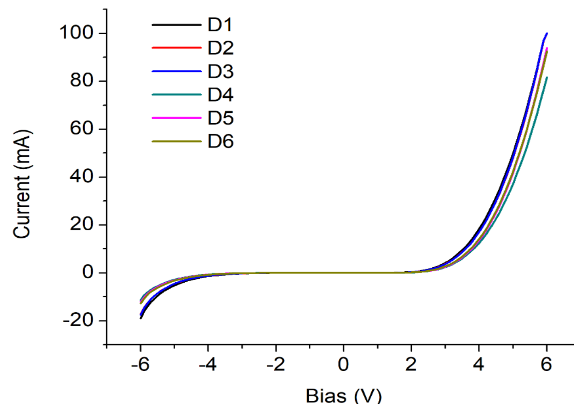


Figure 2. Current vs. bias voltage curves of an $In_{0.34}Ga_{0.66}N$/GaN disk-in-nanowire arrays detectors (D1 to D6 are array of identical test devices fabricated on a process evaluation chip).

Publications and References

[1] Arnab Hazari, Alexander Soibel, Sarath Gunapala, and Pallab Bhattacharya, “Infrared Absorption at 300 K in InGaN/GaN Disk-in-Nanowire Arrays Grown on (001) Silicon”, *IEEE Photonics Technology Letters,* **29**, (Oct 15, 2017): DOI: 10.1109/LPT.2017.2752716