Virtual Research Presentation Conference

Direct Back-End Integration of III-V Single Crystalline Materials on CMOS via Growth for Active Integrated Photonic Components and 3-D Integrated Sensing Technologies

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Program: (SURP)

Jet Propulsion Laboratory
California Institute of Technology

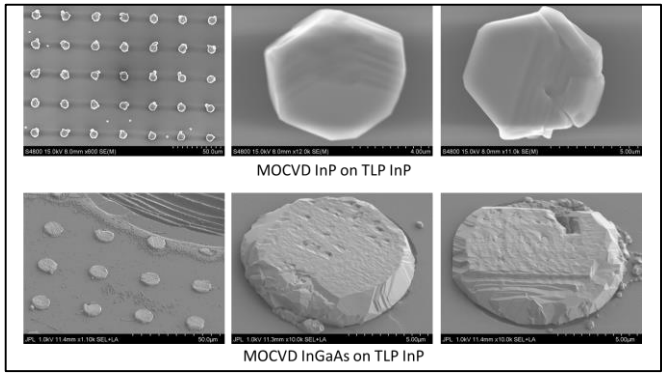
Assigned Presentation #: RPC-197

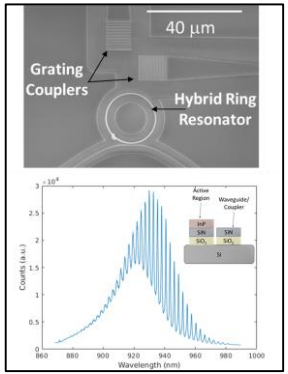
Tutorial Introduction

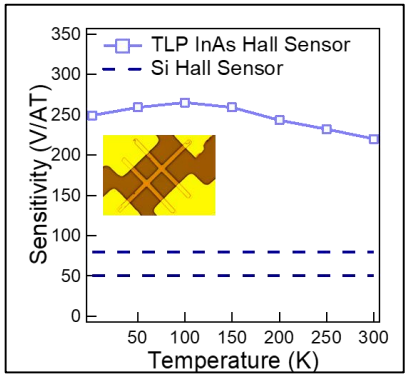
With the end of Moore's Law looming, the semiconductor industry has made a concerted effort to identify and develop pathways to continue performance improvements and functional diversification of platforms. The work under this SURP with USC focuses on addressing the question:

"How can we develop next-generation imaging and sensing devices, focal plane arrays, and technologies?"

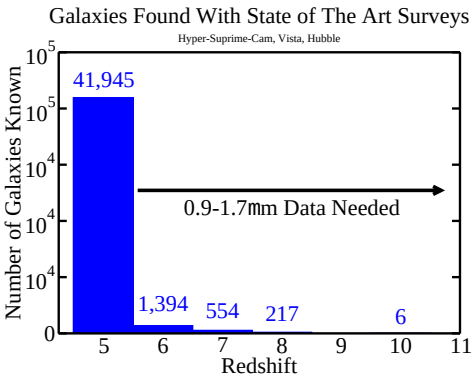
To address this challenge, JPL and USC have been co-developing a new semiconductor growth technique which enables compound semiconductors—materials that have properties complementary to silicon, but are extremely challenging to grow on already completed silicon circuits. Using this new growth technique, we are exploring the possibility of creating focal plane arrays which can potentially achieve higher performance and lower cost than those created by today's state-of-the-art wafer bonding techniques.





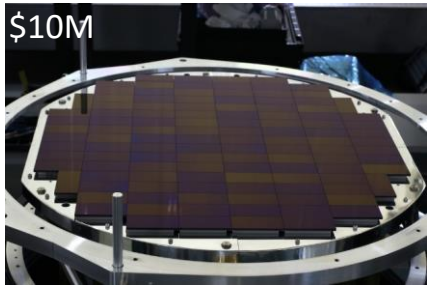


Problem Description

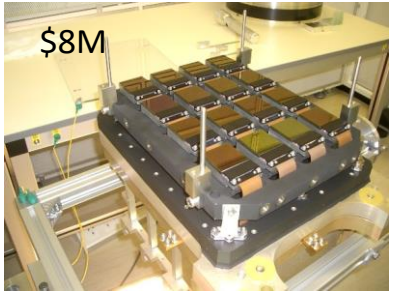


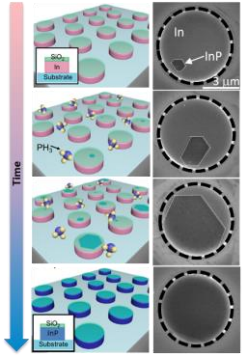
- Cutting edge Astronomy is at >1µm wavelengths
- This is the data needed to find the earliest galaxies that formed and understand how they re-ionized the universe
- This is the darkest part of the sky from space and the best place to do cosmology
- The cost and availability of the detectors is a the limiting factor in building instruments at these wavelengths
- The two cameras below left had similar detector costs despite vast size difference
- TF-VLS enables high quality IR material growth directly on ROICs, eliminating hybridization and substantially reducing cost.
- This new III-V detector fabrication technology will dramatically reduce the cost of SWIR and making very large IR FPAs possible.

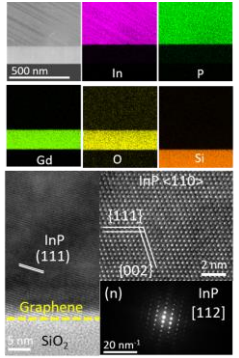
State Of The Art Optical Focal Plane, Hyper-Suprime-Cam
872 Megapixels



State Of The Art IR Focal Plane
VISTA - 67 Megapixels





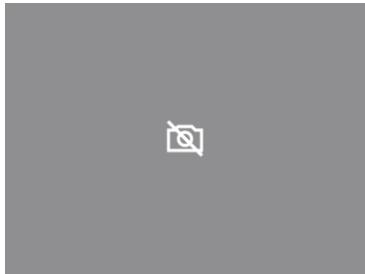


Problem Description

a) Recent developments in non-epitaxial semiconductor growth at USC in collaboration with JPL have made it possible to realize single crystalline III-V films on silicon circuits. There is simultaneously a need for large area, economically feasible, science grade FPAs in the near IR wavelength range.

b) The present day SOA technologies utilize two separate semiconductor wafers to enable functional integration of III-V's with Si circuits. This process is costly, low-yield, and limits the level of integration possible.

c) Relevance to NASA and JPL (Impact on current or future programs)
If successful, this program FPAs populated with extremely low cost, science grade APS IR sensors FPAs would revolutionize the design and development of IR instruments and even world class IR missions such as WFIRST and Euclid. This is potentially enabled by the approach being developed here. For the long term, developing this technology would provide JPL with a strong base that could prove revolutionary for multiple electronic and photonic devices, circuits and systems



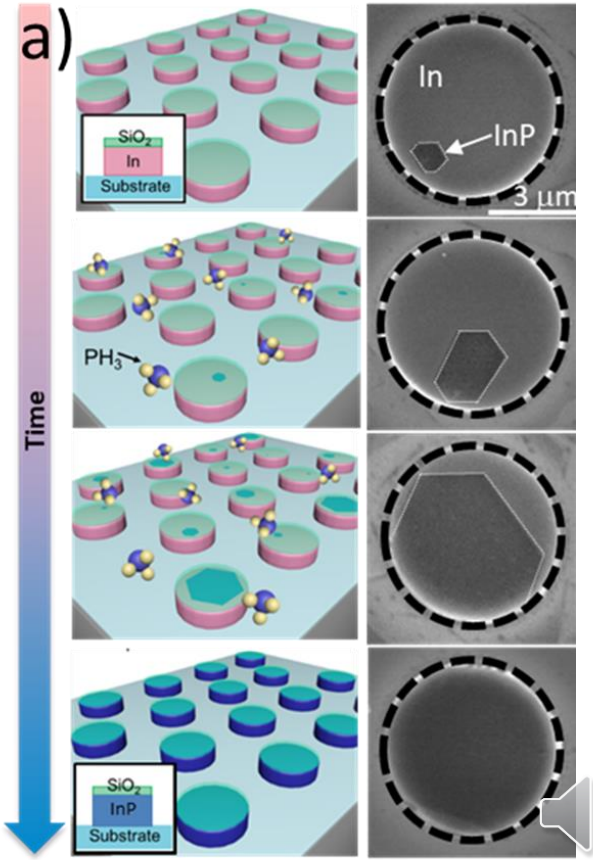
Methodology

a) Approach

A group III metal is first patterned, followed by growth of a single crystal of the III-V material in the desired location. Figure 1a shows the schematic, and side-by-side microscopy experimental results of the single crystals growing via this approach. Here, we will first grow InP single crystals using the TLP approach, and then leverage the well-established MOCVD technology to grow epitaxial layers of lattice matched materials on the TLP InP. This will allow us to potentially create materials with homoepitaxial quality on amorphous substrates. Photodetectors will then be fabricated and characterized from these InP/InGaAs structures.

a) Innovation

Through this approach, we can create local 'virtual substrates' that enable traditional state-of-the-art epitaxial techniques to be utilized on non-epitaxial substrates.



Results

Achevement #1: Grown InAs at back-end compatible temperatures of 300 ºC with room temperature mobility of ~5900 cm^2/V-s. **This is a record high mobility for non-epitaxial materials grown at any temperature.** Modeling illustrates that by reducing the surface roughness of these materials, **room temperature mobilities of ~20,000 cm^2/V-s can be achieved**.

Next Steps: We will leverage the recently demonstrated atomic layer etch process that has demonstrated general smoothing to take the as grown InAs materials and improve the surface roughness to achieve the modeled mobility of 20,000 cm^2/V-s.

Achievement #2: Demonstrated InAs photoconductive SWIR photodetectors with detectivity of >0.5 A/W at 1550 cm^2/V-s directly grown on Si/SiO_2 substrates. These responsivities are similar to commercially available detectors.

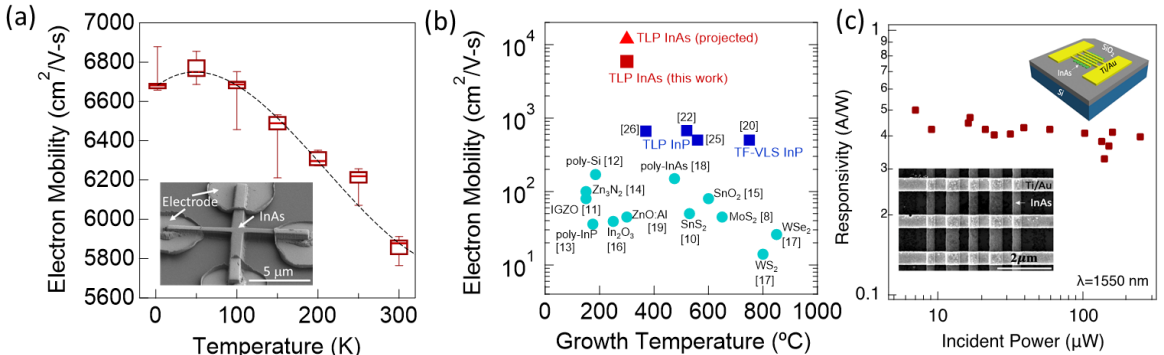
Next Steps: The present devices are simple as-grown photoconductive detectors. Next, we will demonstrate that via back-gating of these devices, the carrier concentration in the InAs can be tuned, enabling suppression of dark current and obtaining high-detectivity InAs devices, with sensitivity for wavelengths below 3.5 mm.

Achievement #3: Demonstrated controlled growth of TLP InP on Si/SiO_2 substrates followed by MOCVD InGaAs selectively on TLP seeds.

Next Steps: Using this technique, we will now proceed with growth of InGaAs p-i-n detecors directly on TLP InP. These structures will directly allow us to test the dark current and responsivity of the desired InGaAs detectors operating at wavelengths <1.7 mm.

Achievement #4: Using Atomic Layer Etching, we have demonstrated that as-grown TLP InP, which exhibited surface roughnesses of ~3-4 nm RMS, could be smoothed to ~1 nm RMS through initial, non-optimized etch conditions.

Next Steps: Using this technique, we will identify whether ultra-smooth integrated photonic structures such as waveguides can be made.



Publications and References

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