Barrier Infrared Detector Digital Focal Plane Arrays

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Objectives: The goal of this project is to demonstrate digital focal plane arrays (DFPAs) using the JPL barrier infrared detector (BIRD) technology. The BIRD enables continuously adjustable cutoff wavelength ranging from the short wavelength infrared (SWIR) to the very long wavelength infrared (VLWIR), and higher operating temperature and/or sensitivity than previously attainable in cost-effective, robust III-V semiconductors. Digital FPA simplifies output electronics and reduces interference in signal chain. FPA based on large-well-depth digital-pixel ROIC (DP-ROIC) provides much higher dynamic range than a conventional FPA, leading to higher operating temperature, potentially reducing cooler size, weight, and power (SWaP) to the benefit of long wavelength infrared (LWIR) and VLWIR instruments for Small Satellites.

Background: The JPL high operating temperature (HOT) barrier infrared detectors and focal plane arrays (FPAs). The HOT-BIRD first saw success in the MWIR (cutoff wavelength $\lambda c \sim 5.5 \mu m$), demonstrating the best characteristics of both II-VI and III-V detectors: HgCdTe (MCT) high operating temperature, and InSb FPA uniformity, operability, large-format capability, and affordability. This has led to strong interests in extending the development to long-wavelength infrared (VLWIR; λc >12 µm). Ongoing (V)LWIR BIRD efforts supported by NASA and DoD have also demonstrated robust high operability & uniformity FPAs. However, longer cutoff wavelength requires more cooling to reduce dark current and maintain signal-to-noise ratio. The concern for space applications is that increased cooling and radiator requirements demand more cryocooling volume, mass, and power. The challenge is particularly acute for spectral imaging applications where lower dark current is needed to accommodate the lower photon flux per pixel. Future small satellite missions will present even more challenges for (V)LWIR FPAs, as operating temperature must be increased so that cooler (and radiator) SWaP can be reduced.

Approach and Results: The signal-to-noise ratio in an infrared FPA can be improved by the size of the storage well capacitor in each unit cell of the readout integrated circuit (ROIC). In the typical (V)LWIR imaging application, due to well-size limitations the integration time is a few tens of milliseconds; this means that most of the available signal (photon flux) is not used. An innovative approach for getting around this problem is to use a digital-pixel ROIC (DP-ROIC) [5], where the well capacitor is reset when filled, and a digital counter built into each unit cell is incremented; this provides a much higher effective well capacity than achievable in a conventional analog ROIC. A digital FPA made with a DP-ROIC permits longer integration times. The benefit of having a higher effective well capacity can be seen in Figure 1, which plots the NEDT (noise equivalent differential temperature) as a function of capacitor well depth for a 30-µm square, 12-µm cutoff detector at various operating temperatures, looking at a 300 K scene in the 10.5-11.5 µm band through F/1.4 optics. The NEDT is the key figure of merit that represents the minimal resolvable temperature difference (smaller the better). We note that in general, lowering the detector operating temperature reduces the NEDT. We also see that as we increase the well depth from 8 million electrons (Me⁻) (typical for conventional analog ROIC), NEDT decreases. It can also be seen readily that for a fixed NEDT value, the attainable detector operating temperature increases with the well depth. For instance, with a 400 Me⁻ well, a 50 mK NEDT can be achieved at 85 K, which is significantly higher than at 70 K for 8 Me⁻ well depth. We have grown long and very long wavelength barrier infrared detector material, and fabricated single-element detectors to verify their performance and suitability for FPA production. We have acquired the digital-pixel ROICs, and have completed the design and acquisition of photolithograph mask set for the digital FPA (see Fig. 2). Figure 3 shows a wafer of fabricated detector arrays, and a hybridized FPA seated and wired bonded to a custom ceramic chip carrier. Figure 4 shows the spectral quantum efficiency measured from FPA processing evaluation chips (PECs) fabricated from two different detector array wafers; the cutoff wavelengths are 10.5 µm and 12.5 µm. We have also put together test setup for digital-pixel FPA characterization, including FPA chip carriers, FPA electronics, and were able to acquire infrared images with the setup. We have also developed a novel infrared detector architecture that enables the reduction of etch depth in focal plane array fabrication. Benefits of this new detector architecture includes the reduction of surface dark currents and 1/f noise, and is especially helpful for long and very long wavelength infrared FPAs. The device architecture has been successfully incorporated in a proof-of-concept focal plan array; an image taken with the 12.3 µm cutoff FPA operating at 70 K is shown in Fig. 5.

Significance/Benefits to JPL and NASA: The higher operating temperature advantage of the BIRD DFPA leads to reduced cryocooling system size/weight/power, thereby enabling infrared instruments for more versatile remote sensing and science data collection endeavors, including for CubeSat/SmallSat-class missions. For NASA Earth Science, 2017 Decadal Survey applications include: Surface Biology and Geology (hyperspectral imagery in the thermal IR), Greenhouse Gases (thermal IR sounders), and Planetary Boundary Layer (hyperspectral IR sounders). In addition, all of our current NASA projects, including CubeSat Infrared Atmospheric Sounder (CIRAS) (InVEST), VLWIR infrared focal plane arrays for Sustainable Land Imaging Technology (SLI-T) (ROSES), with the second se imager (HyTI) for SmallSat platform (InVEST), and Versatile Computational Pixel Infrared Land Imager (SLI-T)

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Fig. 1. NEDT (noise equivalent differential temperature) at various detector operating temperatures as functions of capacitor well depth.

Program: FY21 R&TD Strategic Initiative

Strategic Focus Area: LWIR (to ~15µm) Digital Focal Plane Array (DFPA)





to a ceramic chip carrier.

Fig. 2. (Left) A wafer containing readout integrated circuit (ROIC) chips, and (Right) Mask set design for focal plane detector arrays and process evaluation chips.

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Fig. 3. (Left) Wafer containing fabricated detector arrays and process evaluation chips, and (Right) a focal plane array mount and wired-bonded

Acknowledgements: This task has benefitted from the substantial contributions of Alex Soibel (detector fabrication and characterization), Brian Pepper (material optical characterization), Anita Fisher (detector fabrication) and characterization), Sam A. Keo (focal plane array fabrication), Cory Hill (focal plane array fabrication), Don Rafol (focal plane array characterization) and Yuki Maruyama (focal plane array characterization) of the JPL Instrument Electronics and Sensors Section (389).



Fig. 4. Spectral quantum efficiency of detectors from two different focal plane array process evaluation chips taken at 70 K.





Fig. 5. An image taken with a 12.3 µm cutoff proof-of-concept focal plane array (FPA) build from a new device architecture designed to reduce etch depth in FPA fabrication process.

> **Clearance Number: RPC/JPL Task Number: R19024**