National Aeronautics and Space Administration

Cell Library Assurance for Strong ASICs (Class A)

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Program: FY21 R&TD Strategic Initiative **Strategic Focus Area: Cell Library Assurance for Strong ASICs (Class A)**

Objectives

Develop an **upfront assurance approach** that aims to enable JPL to design and fabricate reliable, radiation tolerant ASICs capable of supporting the bulk of our missions by :

Removing two key factors hindering JPL ASIC implementation in the past 1) specialized cell libraries (radiation hardened cell libraries) 2) in-depth radiation design expertise.

Develop and validate instead

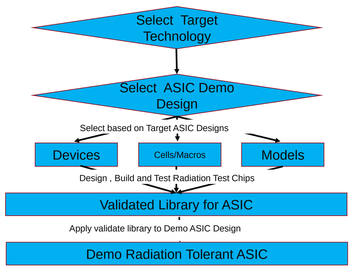
1) Automotive grade library with high reliability of 15-years and high level of process control
2) advanced modern technology
3) an efficient radiation test matrix for the automotive cell library over a series of test chips
4) identifying the preferred library elements in design for radiation guidelines
5) validate potential for first run success in sample design

Background

- Over the last 35 years, we saw miniaturization and automation transforming all aspects of our every day lives with the arrival of cell phones with powerful computing and communication in our hands and smart appliances to handle operations from ordering groceries to water the plants in our homes .
- Such miniaturization and automation (autonomy) represent how advances in electronics can powerfully transform our space systems, but the commercial electronics underlying commercial miniaturization and automation do not have sufficient reliability and space environmental tolerance to be directly inserted into our systems.
- Our missions are still primarily relying on dated but reliable and space tolerant military grade electronics. The performance gap between the two types of electronics is already orders of magnitude and still growing.
- We have to find ways to harness the power of modern electronics & bridge that gap.

Approach and Results

- We intend to make the ASIC design flow as straight forward as the FPGA design flow, resulting in a direct path for a mission to utilize ASIC flow to save on cost and SWaP (size, weight and power). No specialized reliability or radiation experience needed to achieve a first pass fabrication success, because the reliability and radiation mitigation has been implemented at the fabrication level beforehand through this R&TD, along with the circuit and fabrication assurance techniques.
- For the ASIC fabrication, we have strategically chosen the Global Foundries automotive fabrication technology (22FDX) for its many benefits.
  1) The GF 22nm production line is one of the highest volume lines in the global market, guaranteeing the highest yielding, stable production to support the 10+ year product run requirement of the automotive industry.
  2) The technology is offered on silicon-on insulator (SOI) substrate known to be impervious to single event latchup. This characteristic vastly mitigates the most vexing problem in the use of COTS products.
  3) The total ionization dose (TID) capability of this 22nm line is known to be significantly higher than 100 krad(Si), sufficient for most of NASA's missions.
  4) 22nm technology node provides high speed devices and I/Os to support advanced logic functions for future computational requirements while at the same time mature enough to support the range of mixed signal and RF functions that are also key to spacecraft electronics miniaturization.
  5) Monthly shuttles available creates reliable development and design scheduling.
- In FY20, pathfinder test chip was designed and built.
- In FY21, designing second test chip with circuits to quantify heavy ion, laser and ion dose effects
  1) Over 100 structures in design to cover transistor voltage and sizes
  2) digital and analog design flows being exercised
  3) a fully validated input output circuit ring to address weakness of prior test chip
  4) concurrent substrate design for packaging to support high frequency testing appropriate for 22FDX.
  5) Design completion Oct/Nov FY22



Significance/Benefits to JPL and NASA

We have made significant progress toward providing a baseline radiation characterization, cell selection and design for radiation guidelines for the 22nm GF technology in this task to demonstrate the viability of an upfront assurance approach for effective ASIC design to support NASA/JPL missions. The pathfinder test chip 1 validated the design tools and methodologies and the more comprehensive test chip 2 will be providing quantitative radiation characterization for various radiation effects so that radiation-aware design and cell selection methods can be utilized in future NASA/JPL ASIC designs with significantly higher first pass success rate. The methods will be demonstrated in FY23 by a sample validation design.

Publications

[A] "ASIC Flow for Space Radiation Tolerant Components on Commercial Process Technologies- Part 1 Library Validation," accepted for presentation and publication by the 2022 IEEE/ AIAA Aerospace Conference.

[B] "ASIC Flow for Space Radiation Tolerant Components on Commercial Process Technologies- Part 2 Application to High Performance Computing Requirements," accepted for presentation and publication by the 2022 IEEE/AIAA Aerospace Conference.

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Clearance Number:
RPC/JPL Task Number: R20014