National Aeronautics and Space Administration

On-chip Power-combining Networks with Integrated Harmonic Terminations for Highly-efficient, High-power SSPAs

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Program: FY21 R&TD Topics **Strategic Focus Area: RF and Optical Communications**

Objectives

- Demonstrate a design method which provides a solution to simultaneously improving efficiency and output power of microwave MMIC SSPAs
- X/Ka-band characterization of new-gen GaN transistors for JPL/NASA applications
- Design an X-band (FY'21)and Ka-band (FY'22) GaN MMIC

Problem Description

SSPAs are designed either to optimize output power or efficiency
- Harmonic terminations significantly improve power-added efficiency (*PAE)*
- Power-combiners significantly improve output power (P_{out})

→ **Need power-combiners with integrated harmonic terminations**
- Technology which scales the output power of highly-efficient SSPAs

Below are three 10 GHz MMICs, designed on same GaN process [1]

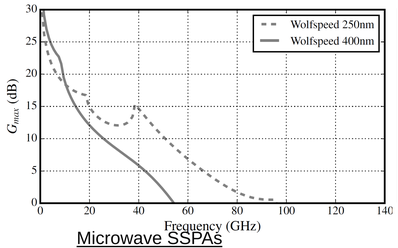
Harmonic terminations: *No
Power combiner: None
P_{out} = 2.5-W , *PAE* = 49%

Harmonic terminations: Yes
Power combiner: None
P_{out} = 2.5-W , *PAE* = 69%

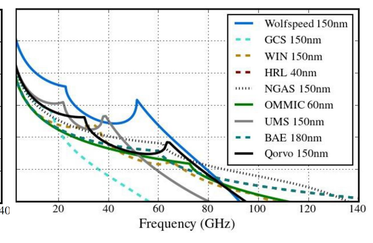
Harmonic terminations: No
Power combiner: Yes
P_{out} = 4-W, *PAE* = 48%

Background

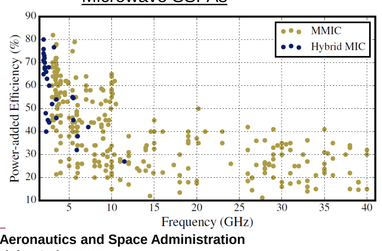
Old-generation GaN (>250nm)

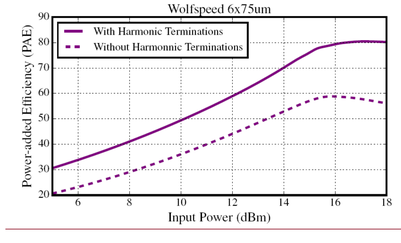


New-generation GaN (<250nm)



Microwave SSPAs





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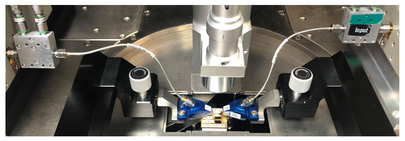
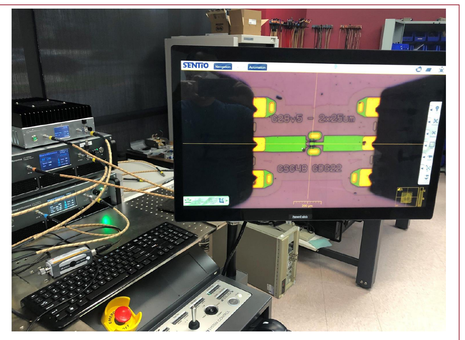
Approach

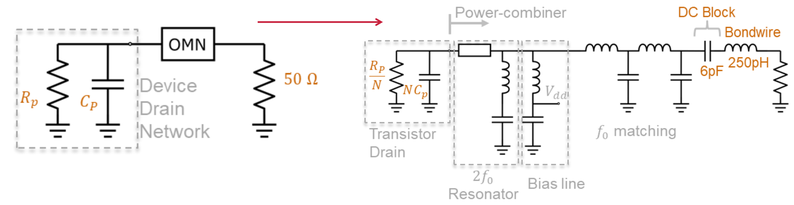
1) On-wafer large-signal X-band multi-harmonic characterization of a bare GaN-on-SiC FET on a new-generation GaN process

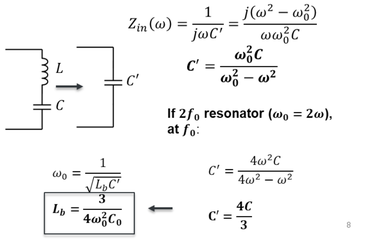
→ **measurement-based design**

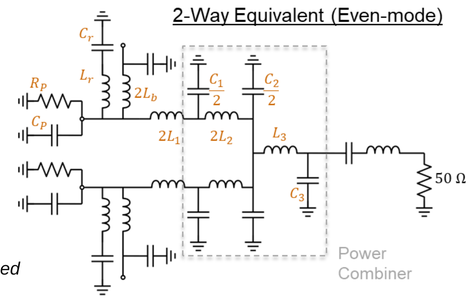




2) Apply innovative design technique (with target load impedance Z_L known)
- Methodically integrates $2f_0$ terminations into an on-chip power-combiner
- Simultaneously co-designs power-combiner, harmonic resonators, DC bias networks, and fundamental matching.
- Can directly scale with number of combined transistors (scale with output power)

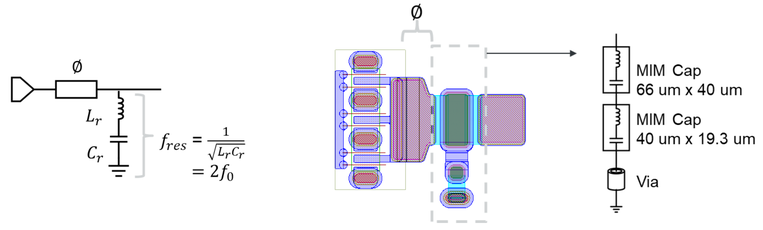






Bias-line inductance to eliminate effective combined capacitance of resonator and transistor drain

3) Realize design on GaN MMIC using design models (electrical and layout) of passive and active components
- Full-wave EM simulations of all passives in GaN/SiC stackup
- Co-simulations with large-signal harmonic balance simulations



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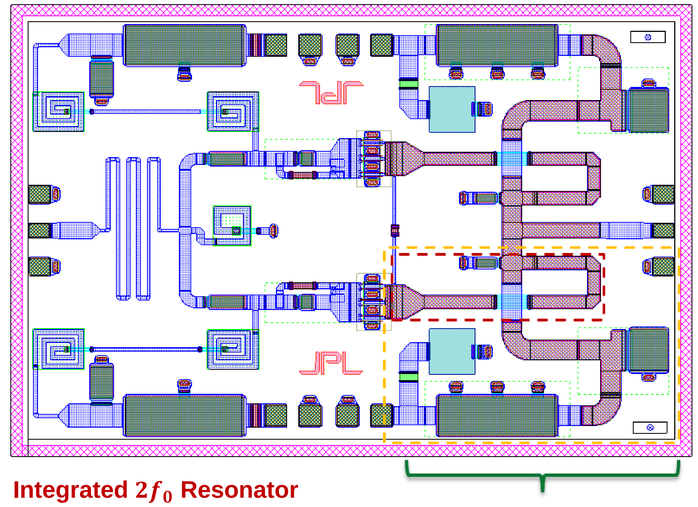
Results

JPL GaN MMIC SSPA for DSN X-band Downlink
New-gen 150nm GaN/SiC process (Wolfspeed)
Chip Size: 3mm x 2mm (compare to λ = 35mm)
Simulated Performance: ***PAE* = 58%, P_{out} = 5 W**
(*Currently being fabricated. Measurements expected Q1 FY22)*



Integrated $2f_0$ Resonator
- Co-designed with Bias line
- Resonates with transistor drain-to-source capacitance to simplify f_0 matching

Bias Line co-designed with $2f_0$ resonator + f_0
- Provides >30dB DC/RF isolation
- Resonates with transistor drain-to-source capacitance to simplify f_0 matching

On-chip Power Combiner
w/ integrated harmonic terminations + f0 matching

Significance of Results

The simulated results of this FY signify that GaN MMICs may now be able to progress the state-of-the-art in terms of power and efficiency, addressing the most challenging technological demands for SSPAs. Technology which simultaneously improves efficiency and output power of solid-state microwave/millimeter-wave electronics has a broad impact on the technical capabilities of many NASA/JPL programs and systems.

References: [1] S. Schafer, M. Litchfield, A. Zai, Z. Popovíc, and C. Campbell, "X-band MMIC GaN power amplifiers designed for high-efficiency supply-modulated transmitters," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, Jun. 2013, pp. 1–3

Clearance Number:
RPC/JPL Task Number: R21113