National Aeronautics and Space Administration

Study of radiation effects on 65 nm circuits with device model integration into industry standard tool chain components.

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Objectives

There are two primary methods for realizing radiation tolerant application specific integrated circuits (ASICs) for use in space environments; starting with a radiation hard semiconductor process or using knowledge of the effects of radiation on the constituent elements to mitigate them at the design level. The former method, although very robust, is costly as it does not take advantage of the economies of scale of common multi-project-wafer (MPW) nodes such as 65 nm. The work discussed here focused on the second approach, where knowledge of radiation effects is applied to the device models for a particular process design kit (PDK). Our objective was to produce new modeling methods, for integrating previously published data on Total Ionizing Does (TID) effects into the simulations, without modifying the native ASIC design tools. We focused efforts on the 65 nm node, as CERN has previously published TID results on this node.

Background

We focused on methods by which we could integrate published TID characteristics on device parameters into the ASIC design environment, without relying on costly modifications to ASIC design software or generation of unique corner files. In doing so we investigated two approaches, one of which we believe is novel and has several advantages over existing approaches in the literature, such as the device wrapper method. This new method allows radiation results to be easily integrated into new and existing designs, is agnostic of the PDK used, and does not require separate schematics to be maintained. It provides JPL a path for designing for TID resilience from the beginning of the ASIC design process. We combined these modeling efforts with TID experiments on a previously designed ASIC, fabricated in TSMC 65 nm to correlate experimental trends with simulation

Approach and Results

We characterized the BGR in the ASIC to TID effects at 5, 25,100, 200, 500, and 1000 krad. A custom PCB was developed (Figure 1), that contained circuitry for both bias during exposure, and characterization circuitry for evaluation. TID data was collected at high and low dose rates, biased and unbiased, to ensure we were observing the correct correlations in trends between experimental and modeled results, that were happening in parallel. These test results are summarized in Figure 3, for both the 1V and 2.5V BGRs that are part of the ASIC.

As existing models were not available, we used previously published TID behavior for the 65 nm node. These publications focused on MOSFET effects due to trapped charge in the surrounding oxide layer, which is known as the Shallow Trench Isolation (STI). TID effects in the gate oxide is negligible for the 65 nm node. There are two separate sets of effects, one associated with narrow channels, radiation induced narrow channel effects (RINCE), and radiation induced short channel effects (RISCE). We focused on modeling of the former in this work, as the devices in the ASIC tested have relatively wide channels, making RISCE essentially zero. RINCE data was fit to a third order, exponential polynomial, the fit vs data shown in Figure 2.

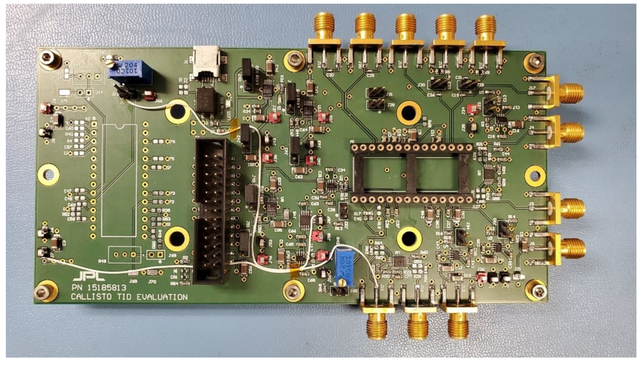

Figure 1. Test board developed for TID exposure and subsequent evaluation. The board shown has only its evaluation (right hand side) populated.

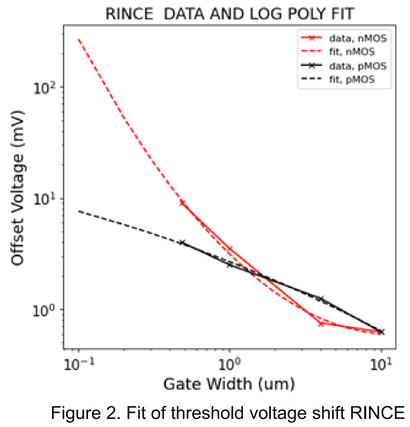

Figure 2. Fit of threshold voltage shift RINCE data at 1 Mrad

The resulting function was then used to model RINCE TID effects using two different approaches. The first was via a “device wrapper” approach, where fictitious DC sources and leakage paths are introduced around the transistor to mimic degradation. The second we termed the “netlist modifier” method, where a copy of the circuit netlist is modified using a custom Python routine. The modified copy of the netlist is then simulated in the Cadence Spectre environment through the use of a second custom script, using OCEAN. Interestingly, we discovered implementation problems with the device wrapper approach. The exponential polynomial created DC convergence problems when using VerilogA to implement the RINCE function. Additionally, this approach requires the maintenance of two separate schematics, one for TID simulation and one for layout generation. The “netlist modifier” method, however, does not suffer from DC convergence problems and does not require a separate schematic to be maintained. It can be used to rapidly evaluate the TID susceptibility of a given design, either retroactively or during the initial design phase.

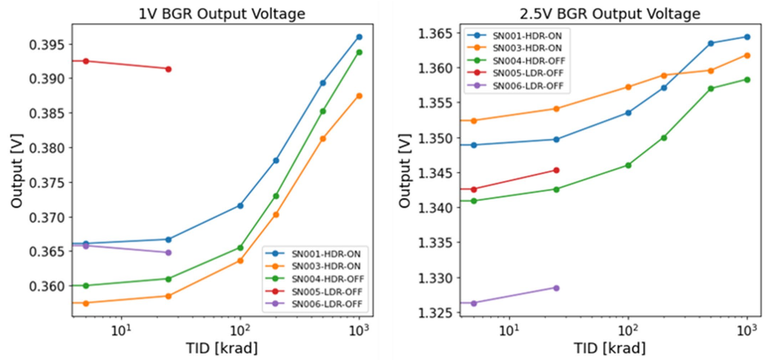

Figure 3. TID test results of the 1V and 2.5V BGRs contained in the ASIC. The low dose rate tests (up to 25 krad) indicate that ELDRS is not at play, the increase in output voltage above 25 krad is most likely due to BJT leakage (not modeled as part of this effort).

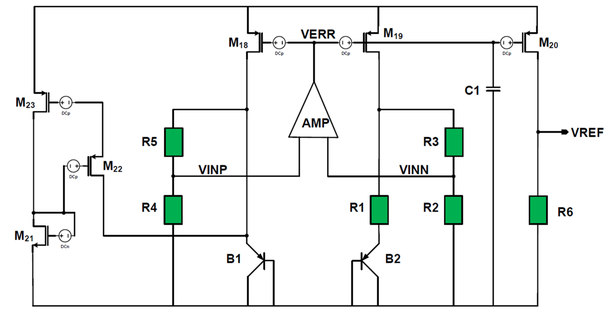

Figure 4. BGR Schematic with RINCE offsets added as DC sources at the gates of each MOSFET for illustration of TID RINCE effects locations. The amplifier in the middle of the diagram is a folded cascode design, also containing RINCE effects.

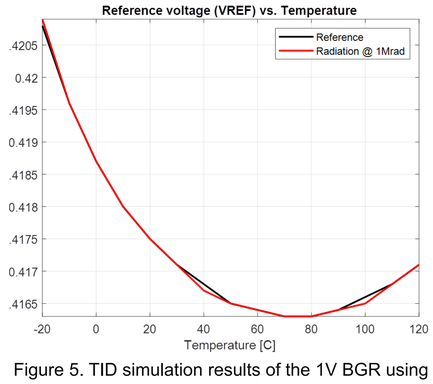

Figure 5. TID simulation results of the 1V BGR using the netlist modifier method. Simulation results predict that RINCE has only a small effect on output performance, mismatches in BJT leakage were subsequently simulated and found to produce higher levels of output voltage variation with total dose.

Significance/Benefits to JPL and NASA

We were able to obtain the objective of developing an approach for easy adaptation of TID effects into the ASIC design flow. This critically impacts ASICs development by JPL and NASA, where evaluation of TID performance must be made at the design phase, but is not currently supported by existing tools. The work from this effort provides a path for such TID evaluation to be made, without expensive design tool modifications. It does require existing experimental data on TID behavior to be available, however. The authors suggest that future ASIC designs contain a set of test structures of constituent elements, routed out to spare pads on the ASIC perimeter. This will allow TID models to be iteratively improved, without dedicating entire runs to device characterization.

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