National Aeronautics and Space Administration

# Analog to Digital Converter for a Phasemeter

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## OBJECTIVES

The objectives of this research are to develop and demonstrate a low power ADC for the JPL ASIC-based phasemeter. The target ADC specification is a bandwidth of more than 50MHz, digitized with an effective resolution of greater than 10bits. The collaboration will support JPL PEMC strategic investment in task "Mixed-Signal ASIC" to develop ASIC capability at JPL. The phasemeter ASIC development aims at technology development for a nanometer accuracy precision laser instrument.

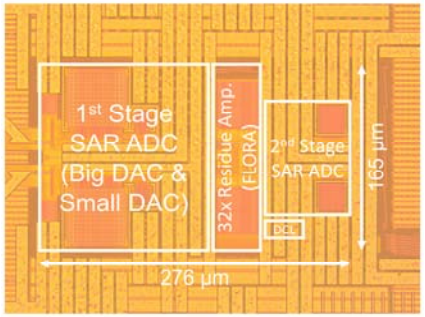


Figure 1: Fabricated Chip Micrograph

## BACKGROUND

- The performance of the ADC limits the overall performance of the phasemeter.
- ASIC implementation promises the most compact and energy-efficient solution This research will research an ADC approach that delivers high performance and is compatible with a ASIC implementation.
- The ASIC approach is difficult as the ADC needs to operate alongside digital circuitry
- SAR-assisted pipeline ADCs have dominated high-performance, high efficiency analog-to digital conversion for more than a decade
- The gain inaccuracy and the power consumption of the residue amplifiers limit pipeline-ADC performance and efficiency

## APPROACH

- The first phase of this project will consider the overall system requirements and choose the optimum ADC architecture
- The next phase of the project will integrate other analog and digital components of the phase meter with the ADC
- A new amplifier is designed to improve the efficiency of the SAR-assisted pipeline ADC
- The fully dynamic floating ring amplifier eliminates need for bias and common mode feedback
- ADC uses 6b 1st-stage SAR ADC, a 32x residue amplifier, a 9b 2nd-stage SAR ADC

## RESULTS

- A prototype ADC is implemented in a 28 nm CMOS process
- The entire ADC consumes 2.7mW from a 1.1V supply when operating at 200MS/s
- Measured SNDR for a low-frequency input signal is 68.9dB

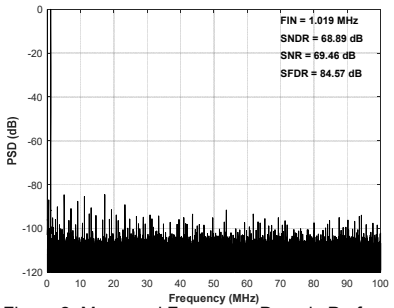


Figure 2: Measured Frequency-Domain Performance

## BENEFITS TO JPL

Significant impact on JPL's capabilities is inherent to this project as JPL will gain insight into high performance ADC designs and obtain the IP for use in JPL's CMOS design library being developed in Mixed Signal ASIC PEMC task. These ADCs and the ASIC IP will make possible significant reductions in power, size and mass of future gravity measurements.

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