National Aeronautics and Space Administration

Direct Back-End Integration of III-V Single Crystalline Materials in CMOS via Growth for Active Integrated Photonic Components and 3-D Integrated Sensing Technologies

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Program: FY21 SURP **Strategic Focus Area: Visible/IR/submillimeter, in-situ and remote sensing instruments**

Objectives

Our objective for this program was to continue to develop our III-V growth technology to demonstrate high quality III-V's on non-traditional substrates that could substantially reduce cost, simplify integration, and improve overall performance. As part of this work, we have studied the growth of InP, InAs, and InGaAs on completely non-epitaxial substrates, the growth of InP on Si substrates, and the smoothing of III-V layers using ALE. Our overarching goal is to then utilize these materials for detectors, sensors and integrated photonic devices.

Background

In this work, we exploring a new III-V growth technology on non-epitaxial substrates can be directed to create a general toolkit for direct heterogeneous 3-D integration of diverse functional units on silicon CMOS circuits. Through the work carried out as part of this proposal, we envision creating a suite of materials and device technologies which would be broadly relevant across JPL Directorates to enable next-generation electronic and photonic systems. Presently, this work is focused on demonstrating high quality, shortwave infrared (SWIR) photodetector devices grown directly on silicon wafers under conditions that would not damage silicon electronic devices (temperatures <450C). The focus of this multi-year proposal is to establish processes for:

(i) III-V detectors, modulators, and light sources directly grown on silicon and silicon nitride waveguides, to allow monolithic III-V active component integration with silicon integrated photonics.

(ii) Heterogeneous integration of multi-modal sensing technologies directly on Si CMOS

Approach and Results

Over the course of the past year, despite the challenges surrounding Covid, we have made considerable progress on both III-V growth and smoothing. One of the major developments is our identification of a new method for direct integration of III-Vs on silicon surfaces to overcome lattice mismatch issues while still growing high quality material.

To enable this, we have used the templated liquid phase (TLP) growth approach that is the core technology studied as part of this proposal and combined it with MOCVD. Specifically, we have taken a silicon (100) wafer, and directly grown InP on this surface using MOCVD. This results in a highly defective, but oriented InP layer. Next, we carry out TLP InP on this substrate. Uniquely, this TLP growth occurs laterally, and as such the majority of defects which are formed in the MOCVD layer are filtered out. Figure 1 shows a schematic of the growth process as well as the final MOCVD growth using the high quality InP layer on Si. Figure 2 shows a cross sectional TEM of the Si-MOCVD InP-TLP InP highlighting the filtering of defects across theMOCVD/TLP interface.

Additionally, we have also studied InAs atomic layer etching. We have shown that materials which started with RMS roughness of ~6 nm can be reduced to ~0.5 nm using the JPL ALE process (see figures 3 and 4). We project that InAs hall bars fabricated using this InAs ALE smoothing recipe will yield substantially higher mobilities, even approaching that of InAs growths onepitaxial substates (see figure 5). Lastly, we have also found that the ALE process for smoothing InAs significantly reduces dark current in some kinds of IR detectors. This new process recipe is now being applied to other programs at JPL for reimbursible sponsors.

Significance/Benefits to JPL and NASA

We project that year 3 of this program will generate single pixel devices that would ultimately enable FPAs populated with extremely low cost, science grade APS IR sensors and would revolutionize the design and development of IR instruments and even world class IR missions such as ROMAN and Euclid. For the long term, developing this technology would provide JPL with a strong base that could prove revolutionary for multiple electronic and photonic devices, circuits and systems. However, beyond this return, the addition of III-V on Silicon Integrated Photonics capabilities, and multi-modal sensing capabilities would be enabling for a broad variety of programs at JPL.

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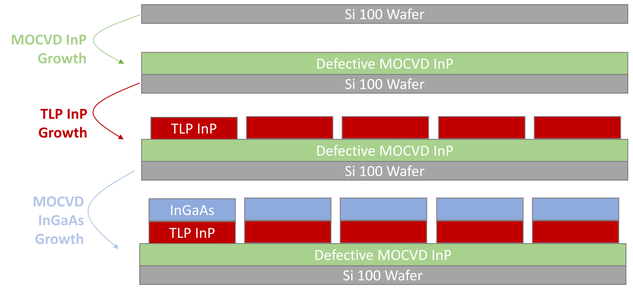

Figure 1. Approach for generating high quality epitaxial templates on non-lattice matched substrate

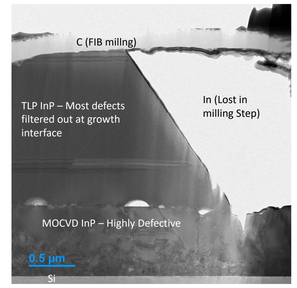

Figure 2. TEM image of Si-MOCVD InP-TLP InP showing the highly defective nature of the MOCVD InP and the near complete filtering of defects into the TLP InP

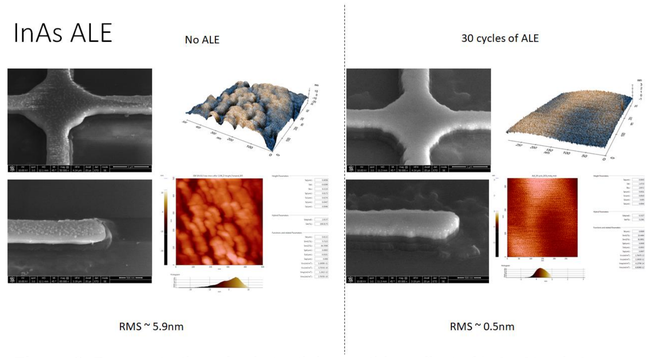

Figure 3. Demonstration of substantial smoothing effect of InAs Atomic Layer Etch process. This smoothing is expected to result in significant improvements in mobility.

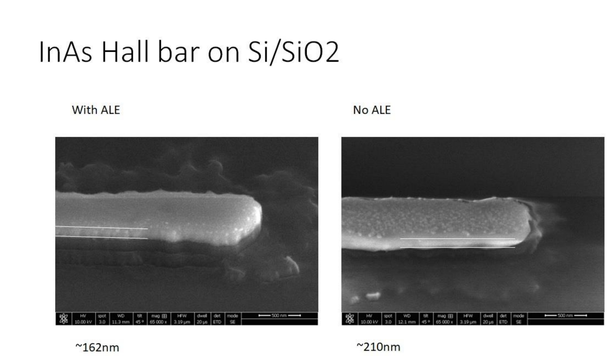

Figure 4. SEM detailing amount of InAs removed by ALE smoothing proces

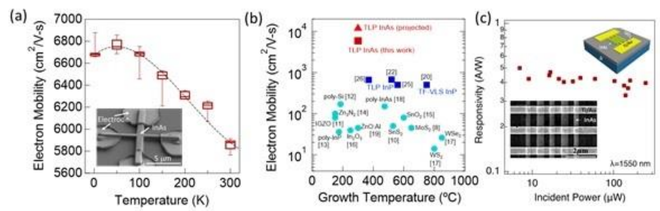

Figure 5. TLP InAs materials and devices. a). Hall mobility vs. temperature for InAs grown directly on oxide at 300C. Inset shows SEM of devices. b). Comparison of our TLP InAs and InP with other non-epitaxial material growth techniques. c). Responsivity vs. incident power for a photoconductive InAs detector on Si/SiO2 substrate. Insets show schematic of device and SEM of fabricated device.

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