National Aeronautics and Space Administration

A CMOS-Molecular-Clock Integrated Platform for Deep Space Communications, Navigations and Radio Science

Principal Investigator: Lin Yi (335); Co-Investigators: Hamid Javadi (386), Alec Yen (Massachusetts Institute of Technology), Ruonan Han (Massachusetts Institute of Technology)

Program: FY21 SURP **Strategic Focus Area: Electronics, Devices and Sensors**

Goals and Objectives

Goal: Investigate and experimentally demonstrate a few key technologies towards a monolithic molecular clock integrated chip with ultra-low power and cost.

1st year objective: Fabricate and characterize a low-loss terahertz silicon micromachined waveguide, which will serve as the gas cell inside the chip-scale molecular clocks (CSMCs).

Background

The concept of a chip-scale molecular clock was conceived by Han's group and later experimentally demonstrated using a standard 65nm CMOS chip and a metal single-mode THz waveguide gas cell [1,2]. By using a CMOS spectrometer to probe the transition frequency of the rotational mode of carbonyl sulfide (OCS) molecules in the low-THz (i.e. 0.1~1THz, 0.23THz in [1,2]) regime, the chip-scale molecular clock offers a time-keeping solution with small size, power, weight, and cost (SWaP-C). TCXOs are the gold standard in most space-borne communications systems in NASA missions. Space qualified Chip Scale Atomic Clocks (S-CSAC) from Microsemi Corp. provide 3x10^-11 stability at 100s integration time with a volume of 16 cm^3. In this proposal, key technologies towards a new, highly miniaturized molecular clock chip will be developed. Such a chip will be used to calibrate the frequency of a TCXO at comparable stability with S-CSAC but with only 0.1 cm^3 addition of volume.

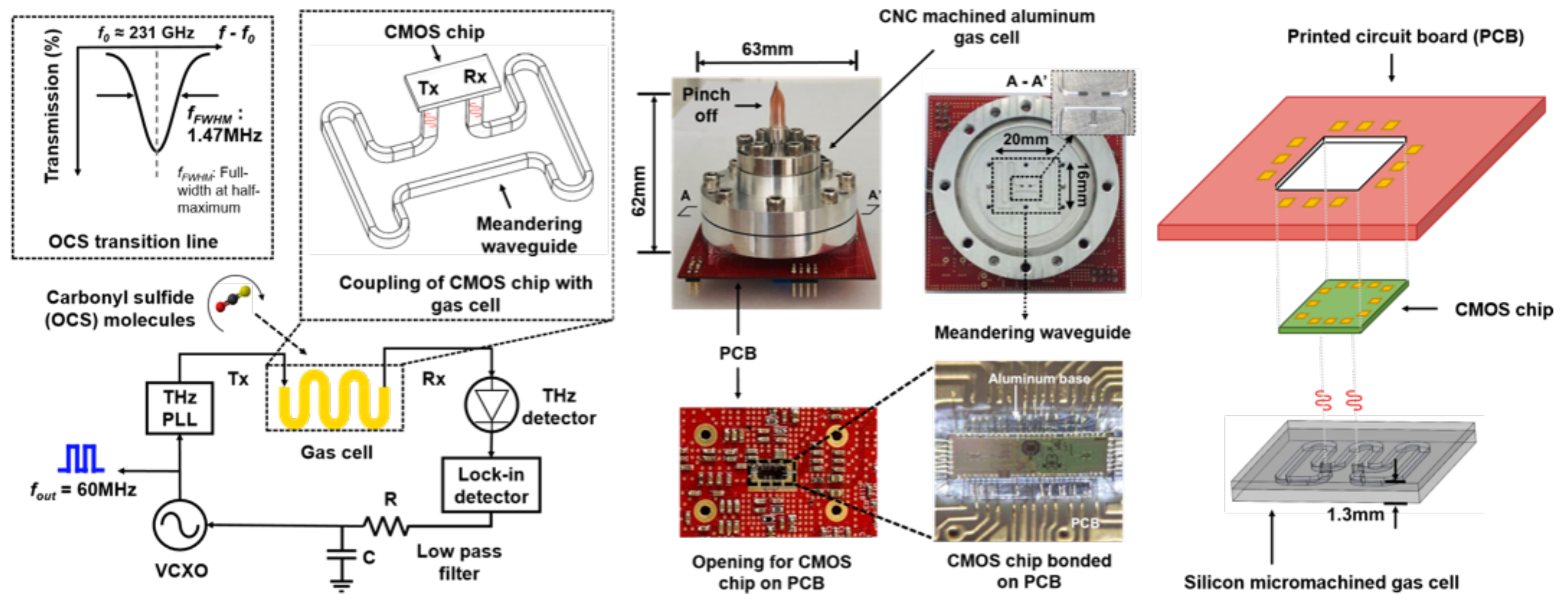

Figure 1. (a) Simplified schematic of the chip-scale molecular clock (CSMC). (b) The previous implementation of CNC machined aluminum gas cell using pinch-off sealing with a volume of ~246 cm3 [3]. (c) Proposed 3D stack using silicon micromachined gas cell

Significance/Benefits to JPL and NASA

This is the first time that the MIT-JPL team created and demonstrated an "all-silicon" waveguide/molecular cell with the consideration of chip-scale clock integration packaging. The 0.27dB/mm loss provides an essential piece of information for future clocks design, and most importantly, the trade-off between required transmitter power, clock performance, size, weight and power, and niche applications. The fabricated all-silicon packageable waveguide serves as the basis for the 2nd and 3rd year effort to achieve high SNR in the molecular spectroscopy.

Publications

Alec Yen, Mina Kim, Lin Yi, Hamid Javadi, Ruonan Han, "Silicon Micromachined Terahertz Waveguide for Miniaturization and Cost Reduction of Chip-Scale Molecular Clocks," submitted to *International Electron Devices Meeting,* San Francisco, CA, 2021.

National Aeronautics and Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

www.nasa.gov

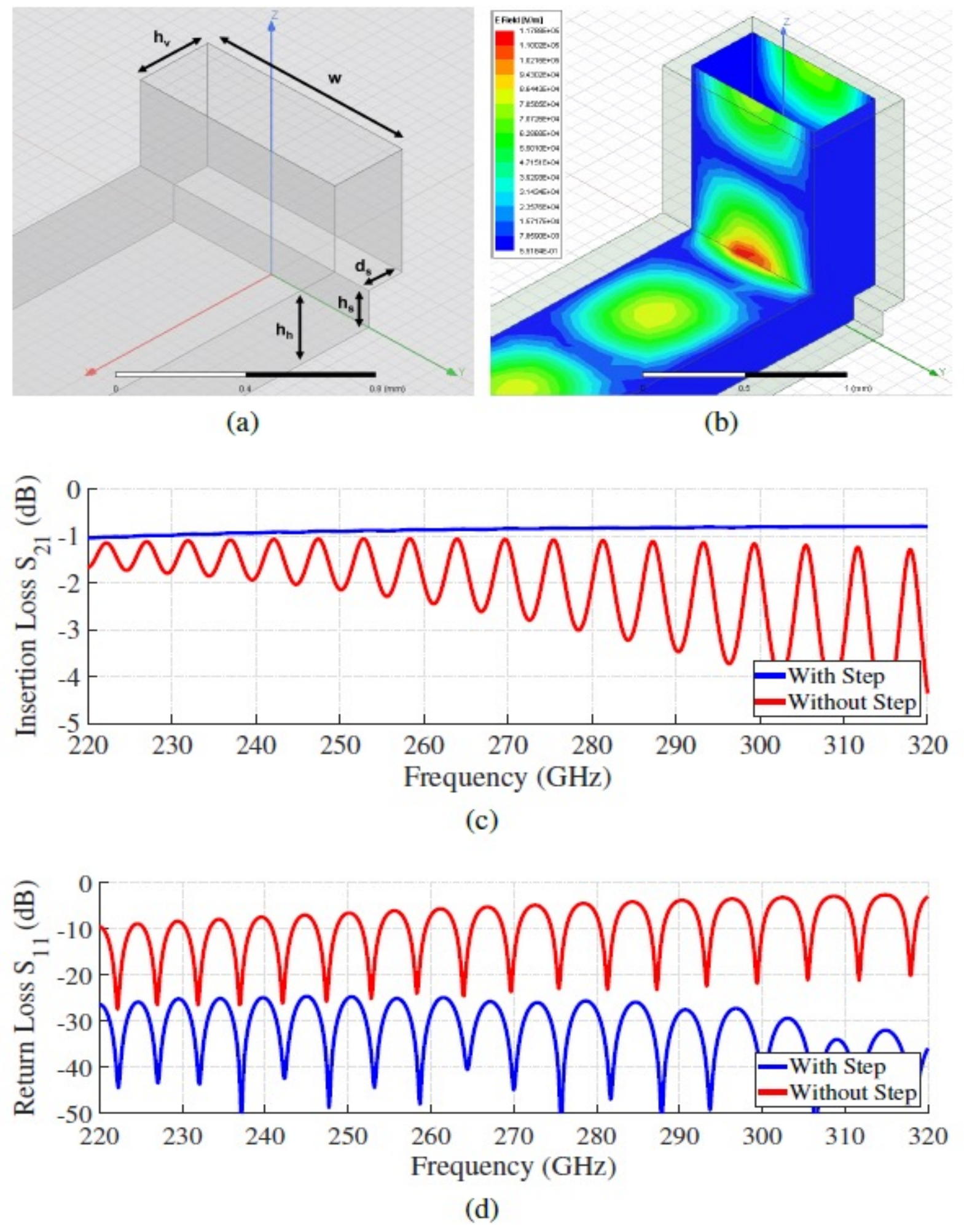

Figure 2. Simulation results. (a) Depiction of waveguide step transition and associated parameters. Final chosen parameters of w=864 μm, h_v=432 μm, h_h=300 μm, d_s=150 μm, h_s=150 μm. If without step transition, h_s=0. (b) Electric field distribution at step transition. (c) S21 and S11 simulation results of a 20 mm-long micromachined waveguide.

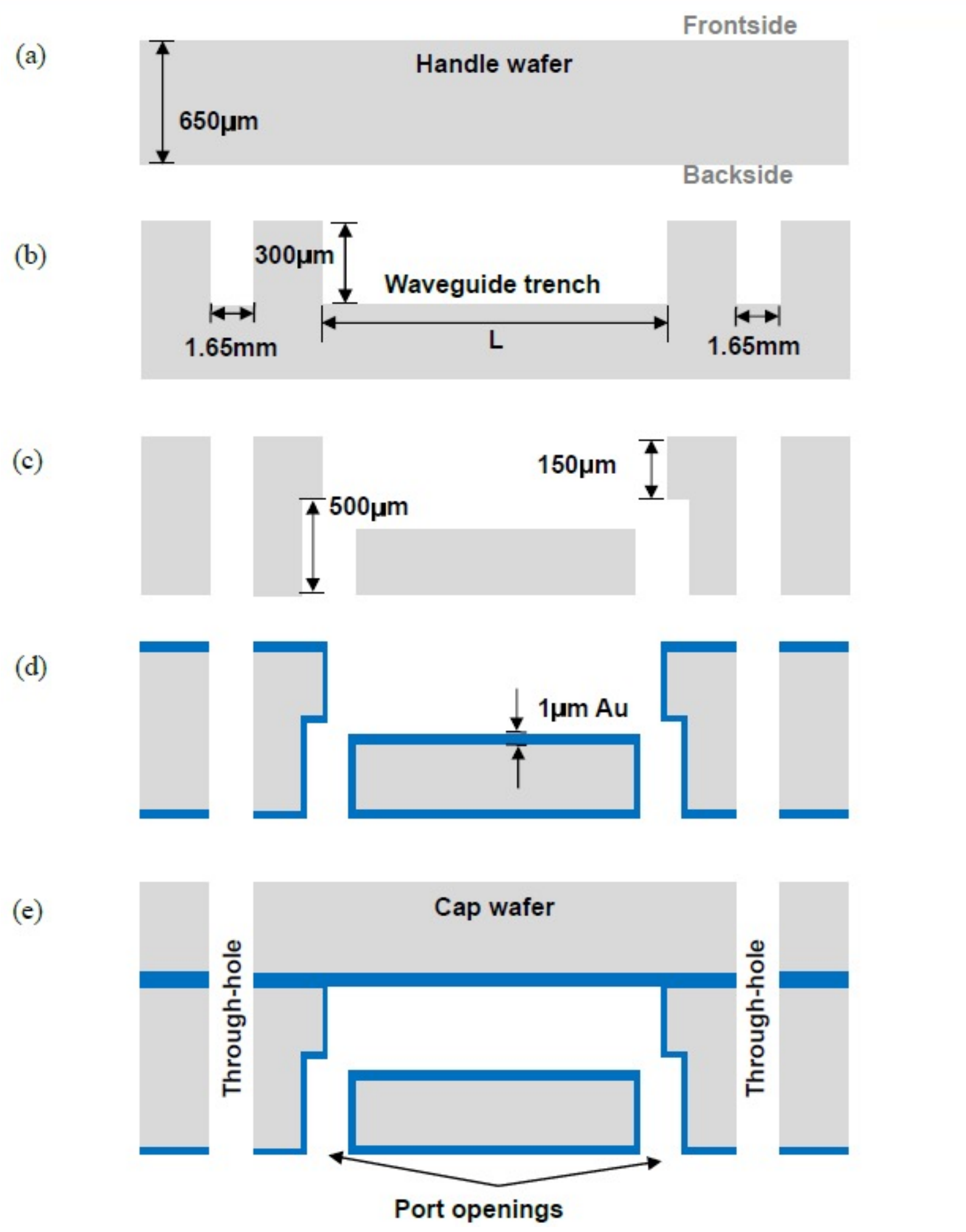

Figure 3. Fabrication process. (a) Bare handle wafer. (b) Frontside DRIE to form trenches and begin through-hole etch. (c) Backside DRIE from to form port openings and step transition bend, and finish through-holes. (d) Metallization by sputtering 1 μm of gold on both sides of the handle wafer and one side of the cap wafer. (e) Thermo-compression bonding with cap wafer.

Approach and Results

The OCS gas was traditionally sealed inside of a CNC-machined aluminum waveguide using pinch-off sealing (Fig. 1b), leading to a large volume of ~246 cm^3, high cost, and unscalable manufacturing. Silicon micromachining is an attractive option for the above goal, as it is common for gases to be sealed inside cavities during wafer bonding. This enables an "all-silicon" clock assembly depicted in Fig. 1c, where the CMOS chip is stacked on top of the gas cell waveguide, introducing a unique need for a pair of waveguide bends to couple to the CMOS chip.

A step transition is used to achieve broadband impedance matching in the waveguide bend. A depiction of the step transition is shown in Fig. 2a. The electric field distribution at the step transition is depicted in Fig. 2b.

The simulated insertion loss S_{21} and return loss S_{11} for a 20 mm-long waveguide are presented in Fig. 2c and 2d. Using the step transition, the simulated $S_{21} > -1.1$ dB and $S_{11} < -25$ dB across the entire 220~320-GHz range. Without the step transition, performance is significantly degraded, as the frequency response demonstrates considerable ripples and increased loss ($S_{21} > -4.5$ dB and $S_{11} < -5$ dB).

The micromachined waveguide is fabricated using two 6" silicon wafers with a thickness of 650 μm. The detailed process is shown in Fig. 3.

Waveguides with and without step transitions were fabricated for comparison. The handle wafer front- and backside are shown in Fig. 4. A waveguide of 3.3 cm in length occupies a volume of just ~0.29 cm^3. This is impressive miniaturization, about 850× smaller than the current CNC machined gas cell (~246 cm^3).

The measured insertion loss is shown in Fig. 5. The average loss of a waveguide with step transition across the 220~320 GHz range is 0.31 dB/mm. At the frequency of interest (231 GHz), the loss of the waveguide with step transition is 0.27 dB/mm. A waveguide without the step transition has more than twice the average loss (0.68 dB/mm). From Fig. 5, the frequency response of the waveguide with step transition demonstrates clear improvement compared to that without a step transition; this is a result of the broadband impedance matching that is introduced by the step.

In summary, during the first-year effort, the MIT team has finalized a preliminary all-silicon based waveguide/molecular cell design with comprehensive and trustful sub-terahertz simulation, developed and demonstrated the fabrication process of such waveguide/molecular cell, and characterized the loss of the waveguide as 0.27dB/mm at 220-320GHz. This leads to a workable ~30dB loss for a typical sample cell in a molecular clock.

PI/Task Mgr Contact
Email: Lin.Yi@jpl.nasa.gov

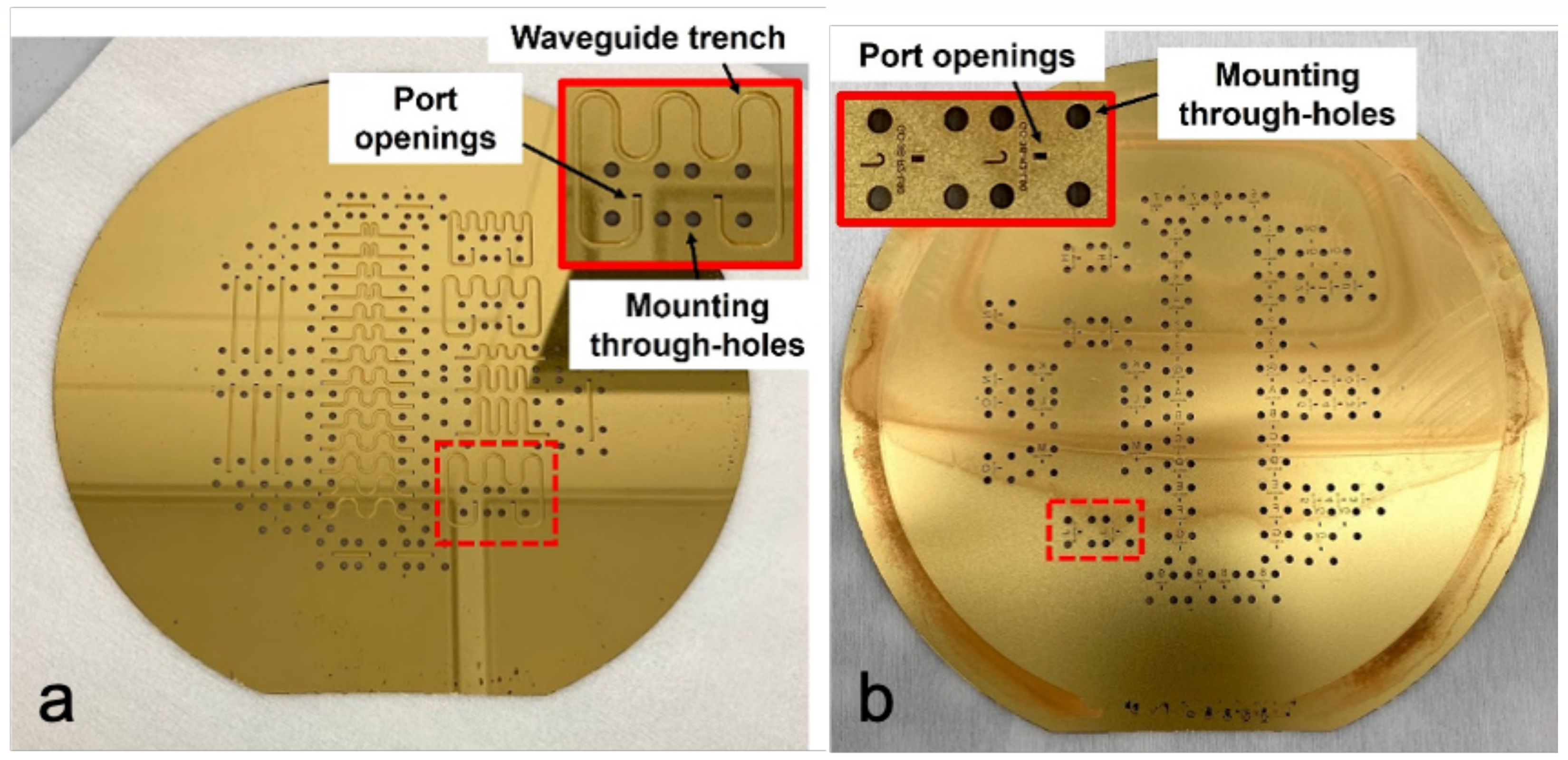

Figure 4. (a) Frontside of handle wafer with waveguide trenches. Inset: meandering waveguide with the shape of the proposed gas cell. (b) The backside of the handle wafer. Inset: close up of port openings and mounting holes.

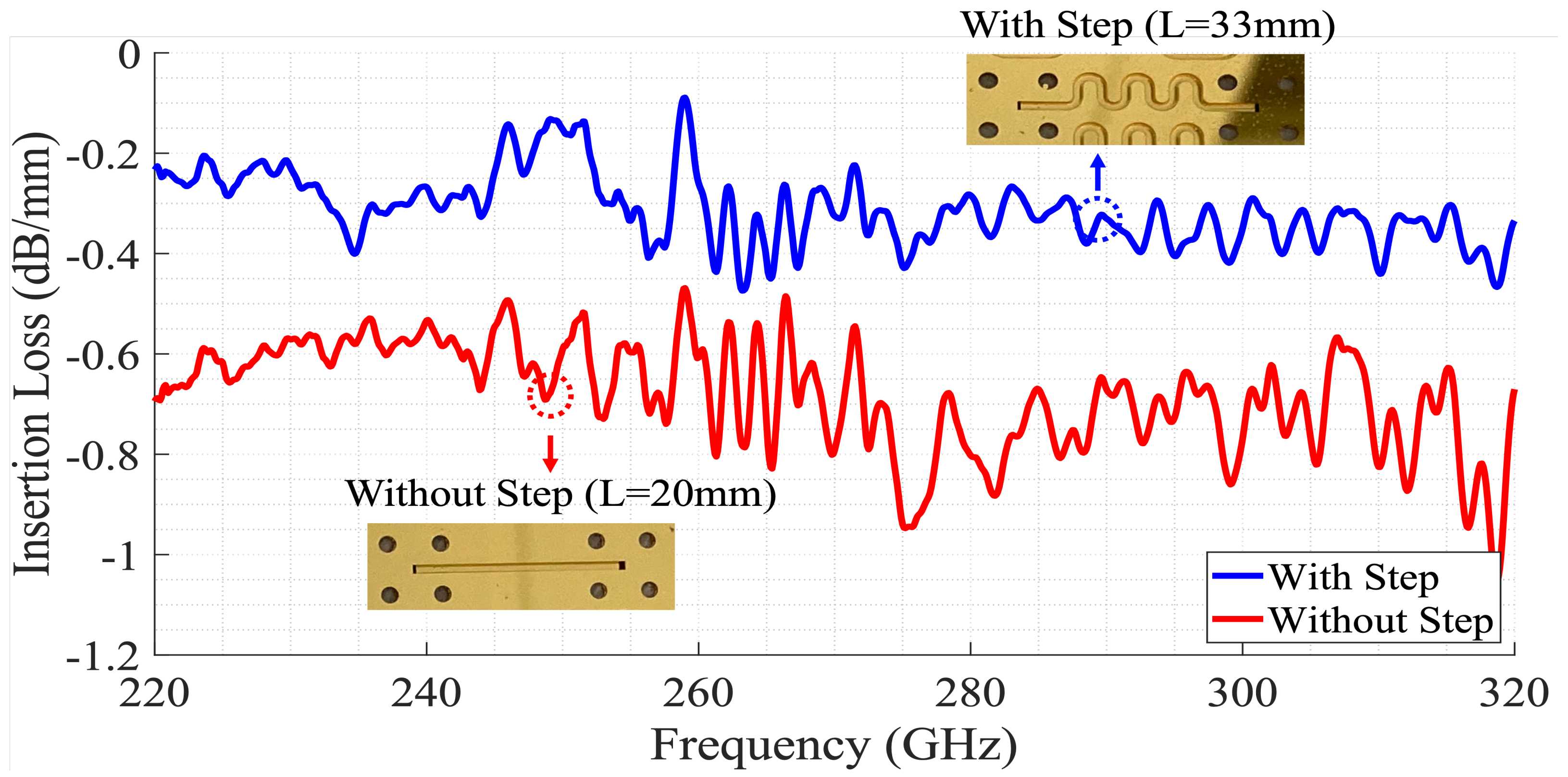

Figure 5. Normalized insertion loss of waveguides with and without step transition.

References

[1]C. Wang, *et al.*, *Nature Electronics*, vol. 1, no. 7, pp. 421–427, 2018.
[2] ——, "Chip-Scale Molecular Clock," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 914–926, 2019.
[3] C. Wang, *et al.*, *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 566–580, 2021.
[4] B. Beuerle, *et al.*, *IEEE Trans. THz Sci. Technol.*, vol. 8, no. 2, pp. 248–250, 2018.
[5] A. Jam, *et al.*, *IEEE Trans. THz Sci. Technol.*, vol. 4, no. 4, pp. 515– 522, 2014.
[6] C. Jung-Kubiak, *et al.*, *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 5, pp. 690–695, 2016.
[7] K. M. K. H. Leong, *et al.*, *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 4, pp. 998–1005, 2012.
[8] T. J. Reck, *et al.*, *IEEE Trans. THz Sci. Technol.*, vol. 4, no. 1, pp. 33–38, 2014.

Acknowledgements

This work is supported by Jet Propulsion Laboratory and the MIT Jacobs Presidential Fellowship. The authors would like to thank J. Scholvin, D. Ward, J. del Alamo, J. Michel, S. Poesse, A. Vardy, and N. Monroe for helpful discussions and suggestions, and MIT.nano for its facilities and equipment. The PI sincerely acknowledges Imran Mehdi, Andrey Matsko, Jon Hamkins, Todd Ely, and Robert Tjoelker for their technological supervisory and mission requirement suggestions.

Clearance Number: 21-4420
RPC/JPL Task Number: SP21005