National Aeronautics and Space Administration

Cell Library Assurance for Strong ASICs (Class A)

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Program: FY22 R&TD Strategic Initiative **Strategic Focus Area: Cell Library Assurance for Strong ASICs (Class A)** **Leader: Harald Schone**

Objectives

Develop an **upfront assurance approach** that aims to enable JPL to design and fabricate reliable, radiation tolerant ASICs capable of supporting the bulk of our missions by :

Removing two key factors hindering JPL ASIC implementation in the past 1) specialized cell libraries (radiation hardened cell libraries) 2) in-depth radiation design expertise.

Develop and validate instead

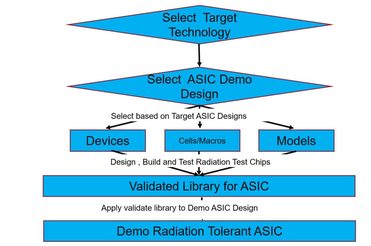
1) Automotive grade library with high reliability of 15-years and high level of process control
2) advanced modern technology
3) an efficient radiation test matrix for the automotive cell library over a series of test chips
4) identifying the preferred library elements in design for radiation guidelines
5) validate potential for first run success in sample design

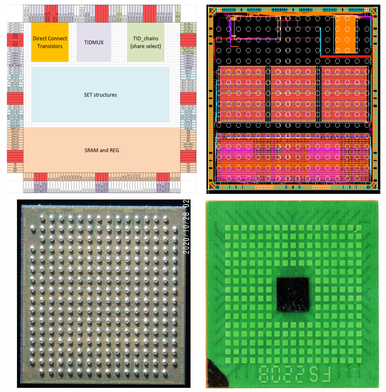
Background

- Over the last 35 years, we saw miniaturization and automation transforming all aspects of our every day lives with the arrival of cell phones with powerful computing and communication in our hands and smart appliances to handle operations from ordering groceries to water the plants in our homes .
- Such miniaturization and automation (autonomy) represent how advances in electronics can powerfully transform our space systems, but the commercial electronics underlying commercial miniaturization and automation do not have sufficient reliability and space environmental tolerance to be directly inserted into our systems.
- Our missions are still primarily relying on dated but reliable and space tolerant military grade electronics. The performance gap between the two types of electronics is already orders of magnitude and still growing.
- We have to find ways to harness the power of modern electronics & bridge that gap.

Approach and Results

- Owing to their tailor-made designs, ASICs can offer significant advantages over commercially available microelectronics in the areas of size, weight, and power (SWaP). However, ASIC development poses several non-trivial difficulties and– while often desired by projects– it is currently seen as an impractical option. **Those difficulties in mind, our intent with this initiative is to refine the ASIC design flow within JPL to something as straight forward as the FPGA design flow, such that missions may have a direct path towards ASIC development and utilization.**
- For the ASIC fabrication, we have strategically chosen the Global Foundries automotive fabrication technology (22FDX) for its many benefits.
    1) The GF 22nm production line is one of the highest volume lines in the global market, guaranteeing the highest yielding, stable production to support the 10+ year product run requirement of the automotive industry.
    2) The technology is offered on silicon-on insulator (SOI) substrate known to be impervious to single event latchup. This characteristic vastly mitigates the most vexing problem in the use of COTS products.
    3) The total ionization dose (TID) capability of this 22nm line is known to be significantly higher than 100 krad(Si), sufficient for most of NASA's missions.
    4) 22nm technology node provides high speed devices and I/Os to support advanced logic functions for future computational requirements while at the same time mature enough to support the range of mixed signal and RF functions that are also key to spacecraft electronics miniaturization.
    5) Monthly shuttles available creates reliable development and design scheduling.
- In FY20, pathfinder test chip was designed and built.
- In FY21& FY22 a second test chip was built, with circuits to quantify heavy ion, laser and ion dose effects
    1) Over 100 structures designed to cover transistor voltage and sizes.
    2) Both digital and analog design flows being exercised.
    3) Fully validated input output circuit ring, addressing the weakness of test chip 1.
    4) The packaging substrate supports high frequency testing appropriate for 22FDX.
- Initial TID testing has been completed on the TID MUX test structure in the second test chip.
- SEE testing has been conducted on the shift registers of the second test chip.
- The TID testing for the SRAM, and shift register is scheduled to complete in before the end of the FY.





From the top-left, clockwise:
1. Planned design of input output and structure placement on test chip 2.
2. Layout structure placement of test chip 2.
3. The fabricated die of test chip 2.
4. The die attached to the substrate.

Significance/Benefits to JPL and NASA

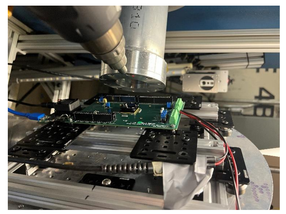
We have made significant progress toward providing a baseline radiation characterization, cell selection, and set of radiation design guidelines for the 22nm GF technology, with the goal of demonstrating the viability of an upfront assurance approach for effective ASIC design in support of NASA/JPL missions. The pathfinder test chip 1 validated the design tools and methodologies and the more comprehensive test chip 2 has been providing quantitative radiation characterization for key ASIC design structures so that radiation-aware design and cell selection methods can be utilized in future NASA/JPL ASIC designs with significantly higher first pass success rate. The methods will be demonstrated in FY23 by a sample validation design.

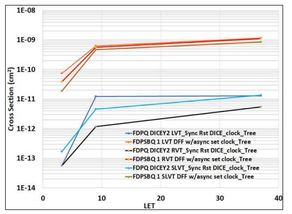
Publications

[A] J. Yang-Scharlotta et al., "ASIC Flow for Space Radiation Tolerant Components on Commercial Process Technologies— Part 1 Library Validation," 2022 IEEE Aerospace Conference (AERO), 2022, pp. 1-10

[B] S. M. Guertin, L. T. Clark, J. Yang-Scharlotta, C. S. Young-Sciortino and J. D. Butler, "ASIC Flow for Space Radiation Tolerant Components on Commercial Process Technologies-Part 2 Application to High Performance Computing Requirements," 2022 IEEE Aerospace Conference (AERO), 2022, pp. 1-11

[C] "A Transistor Array for Extracting Total Ionizing Dose Threshold Voltage Shifts," accepted for publication by the IEEE International Integrated Reliability Workshop.





Left: The SEE test setup.

Right: DICE (blues) vs asynchronous reset (oranges) FFs. Over all, the DICE are harder, but hardness varies by type.

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Clearance Number: URS311635
RPC/JPL Task Number: R20014