National Aeronautics and Space Administration

On-chip Power-combining Networks with Integrated Harmonic Terminations for Highly-efficient, High-power SSPAs

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Strategic Focus Area: RF and Optical Communications

Objectives:

The objective of this work is to demonstrate a design method which provides a solution to simultaneously improving efficiency and output power of microwave and millimeter-wave monolithically-integrated circuits (MMIC) solid-state power amplifiers (SSPAs). At the MMIC level, planar on-chip power-combining of at least 2-10 transistors in the final stage is necessary to achieve output powers relevant for JPL/NASA applications (1-10 Watts). Typical MMIC output stages may use these combiners as part of the matching network, however there currently is no solution on how to also present the the necessary harmonic impedances to each device in the final stage that would maximize efficiency. This is a big reason why, traditionally, high-frequency MMICs/SSPAs are designed to be either high-power (through power-combining multiple transistors) or high-efficiency (single transistor with harmonic resonators).Using the proposed innovative design methodology, multiple microwave power transistors are simultaneously power-combined (to maximize output power), fundamental-matched (to maximize power transfer), and harmonically-terminated (to minimize DC power); all within a single, compact network.This is to be demonstrated on-chip, monolithically with new-generation millimeter-wave Gallium Nitride semiconductors. To demonstrate potential for high-TRL transmitters/instruments, the objective of this work is to deliver two 5-W MMIC SSPAs, X- and Ka-band, with SotA efficiencies.

Background:

In solid-state power amplifiers (SSPAs), there is a known trade-off between output power and efficiency. For both spaceborne and terrestrial NASA applications, both power and efficiency must be maximized. Due to the significant technical challenges involved with designing high-frequency (X-, K-, and Ka-band), high-efficiency, and high-power SSPAs; the current state-of-the-art SSPAs do not perform well enough for the increasingly ambitious NASA missions of the coming decade. Solid-state technology is expected to play an important role in future missions (landers, rovers, SmallSats/CubeSats, distributed platforms, swarms, ground-station transmitters, etc.). In order to advance the state-of-the-art in accordance with proposed missions, JPL Strategic Technologies program, and the NASA Technology Taxonomy, technological advancements are needed in the field of solid-state nonlinear circuit design.

Waveform-shaping is the most effective method of improving transistor efficiency without sacrificing significant output power for SSPAs at frequencies above >3GHz. This technique involves designing structures in the transistor load network to reflect 2^{nd}/3^{rd} harmonic waveforms back into the drain of the transistor (so-called “harmonic terminations”), which serves to significantly improve efficiency. Power-combiners serve to significantly improve output power. There is currently no technology which both power-combines fundamental power and reflects harmonic power.

Approach and Results:

The most effective method for improving the efficiency of a non-linear device while maintaining high output power at microwave frequencies is to reflect the generated 2nd and 3rd harmonic power back into the device so that the device-internal voltage and current waveforms are shaped in such a way that reduces power dissipation. The electrical advantage provided by GaN is that the nonlinearities of the semiconductor, in addition to the low output capacitance and high gain at harmonic frequencies, results in significant harmonic content that can be used to achieve waveform shaping. The advantage provided by MMICs is the precise control of the phase and magnitude of harmonic impedances at the transistor, whereas off-chip harmonic control is significantly limited by large parasitic loss and reactance at microwave/millimeter-wave frequencies due to transitions and the necessary use of lumped elements.

The innovative development of the proposed design methodology on-chip network simultaneously 1) power combines multiple transistors, 2) presents optimal 2nd/3rd harmonic impedances to every power-stage transistor to maximize efficiency, 3) provides fundamental matching, and 4) provides DC-bias for every final-stage transistor; all within a single, compact network. In contrast, traditional design approaches require separate networks for each of the above-listed functions. Although some MMICs do use the output combining stage for partial matching, the challenge of presenting optimal 2nd/3rd harmonic impedance to every final-stage transistor has yet to addressed. This work will demonstrate how this can be achieved by incorporating on-chip structures into the output network that are highly-reflective and precisely phased at harmonic frequencies while also contributing to fundamental matching. In doing so, the entirety of the MMIC, including the bias-lines, parasitic reactances, and the active loading of each final-stage transistor, is leveraged into the multi-harmonic power combing matching network. Additionally, this was consequently seen to eliminate the need for use of lumped elements in the matching network, which even further reduced size and efficiency. Since harmonic terminations are incorporated into the combiners, this method scales effectively with number of combined transistors (output power) and frequency, and can also be applied to the matching networks between PA stages to further improve efficiency.

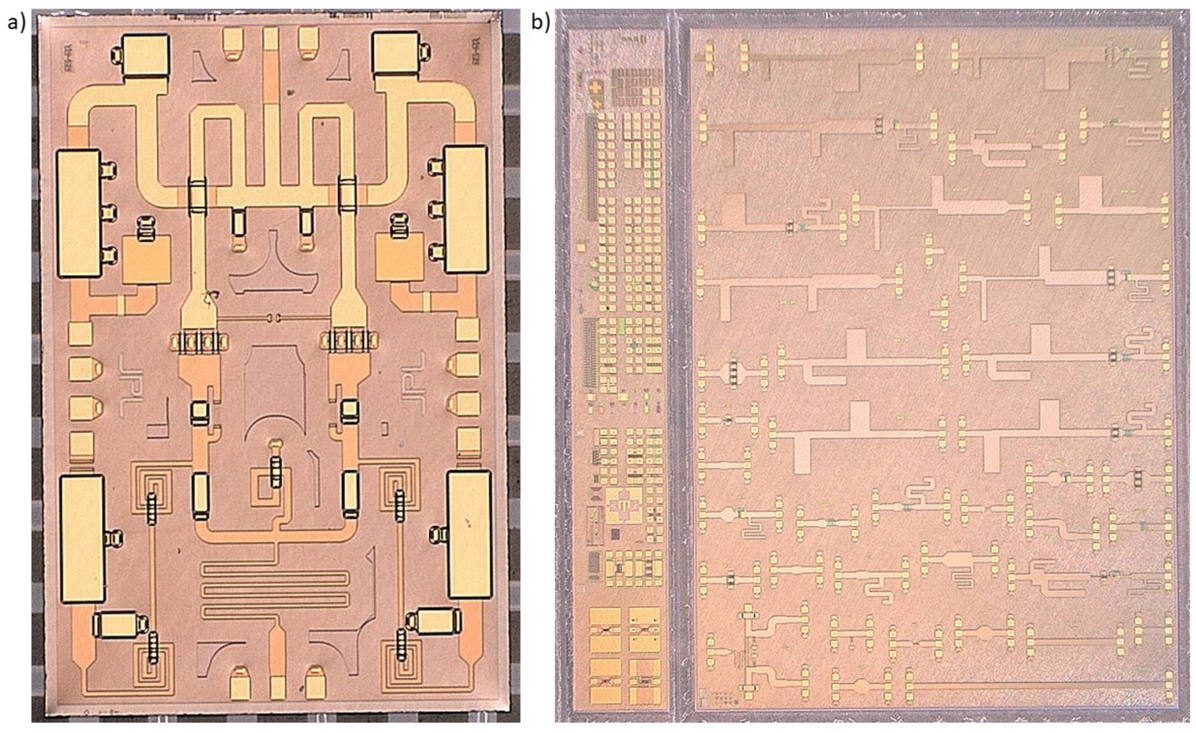

Figure 1. a). JPL-custom GaN MMIC SSPA for DSN X-band Downlink, designed using the described innovation and fabricated on Wolfspeed's 150nm GaN process, with a Sillicon Carbide carrier for enhanced thermal performance. Chip Size: 3mm x 2mm (compare to λ = 35mm). Simulated Performance: PAE = 58%, P_out = 5 W, to be measured in FY23. b). Successful fabrication of a GaN-on-SiC wafer, custom-designed for fundamental and harmonic large-signal characterization of transistors on the newest generation of GaN technology (150nm gate length). Simulations show that if the 2nd harmonic is reflected at a high magnitude and with a precise phase, these transistors will exhibit a power-added efficiency of 65% at 32 GHz (compare to previous generation transistors which measure <30% at the same frequency). However, there exists no technology that is able to effectively characterize (in measurement) transistors at the 2nd harmonic of 32 GHz. Shown is a chip that enables harmonic characterization of Ka-band power-transistors, to inform the future design of a highly-efficient 32-GHz SSPA (expected in FY23); as well as informing JPL on the output-power capabilities of modern GaN transistors for applications ranging in frequency from 3-53 GHz.

Significance:

In year 1 of this task, an X-band GaN MMIC was successfully designed and fabricated (Fig. 1) using the described innovation, leading to a Caltech patent. This MMIC SSPA, custom designed for DSN's X-band Downlink channel, is simulating an output power and efficiency that, if infused into an X-band spatial combiner (measured 92% efficiency) and a power supply (assume 90% efficiency), could lead to a 40-W GaN X-band SSPA with 48% efficiency. The current solution for flight is a General Dynamics GaAs SSPA with efficiency=28%, Pout = 17-W.

In year 2, a novel method for measurement-based efficiency characterization for Ka-band transistors was developed (where previously, harmonic characterization at this frequency has largely been an unsolved problem). This has led to the successful fabrication of a chip designed for the purposes of understanding GaN at JPL frequencies of interest (Fig. 2), and to directly inform the design of the final Ka-band MMIC SSPA deliverable (ensuring lower design risks and unprecedented optimization).

An impactful aspect of this work lies in the progress being made in measuring/analyzing the behavior and performance of the new-generation of microwave/millimeter-wave semiconductors, at frequencies and in applications that are among the cutting edge of the field.

New Technologies:

NTR 52082 "Power-combiners with integrated second-harmonic terminations and fundamental matching".

NTR 52496, "Harmonic characterization of Ka-band transistors using fundamental-only impedance tuners"

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Provisional patent on 7/27/22 (CIT 8721-P)
“High-power solid-state microwave combining technology for deep space communications”, submitted to LSIC Fall Meeting 2022.

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