National Aeronautics and Space Administration

High-Performance Fault-Tolerant Compute Element for Planetary Science Missions

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Program: FY22 R&TD Strategic Initiative.
Strategic Focus Area: High-performance Fault-tolerant Compute Element for Next Decadal Planetary Science Missions. Strategic Initiative Leader: Satish K Khanna

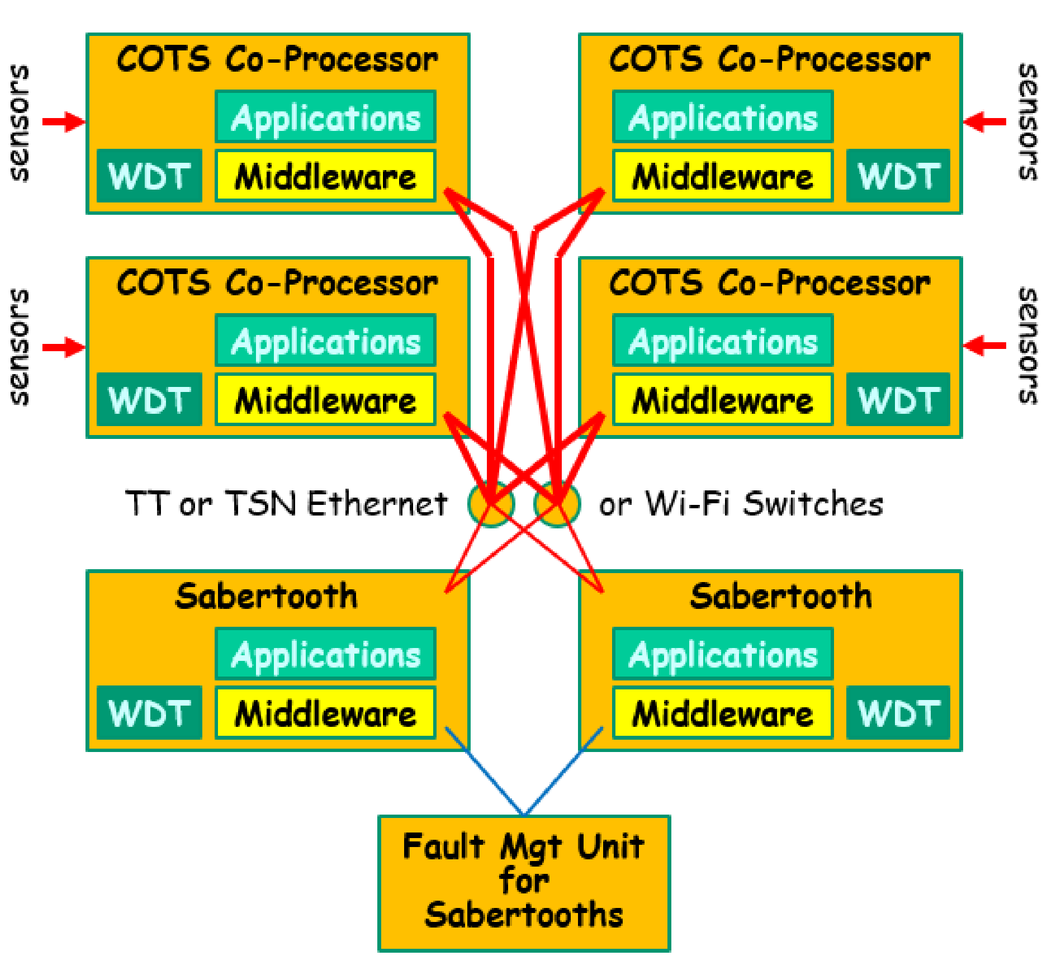
Objectives: To develop a Compute Element that delivers both the latest-COTS computing performance, and the high reliability required for inter-planetary flagship spacecraft. This will be achieved by using a space-grade computer to manage multiple high-performance but low-cost Systems-on-Chip as co-processors, of which several may fail, without harming the mission (= a form of N-Modular Redundancy). The specific objectives for this Compute Element are

i. fail-operational capability despite 2 co-processor failures and/or data-network failures,

ii. computing performance at least 4,000 times that of a traditional Rad750 processor, and

iii. a small SWaP footprint (e.g. < 30W).

Background: The Planetary Science Directorate is currently formulating the next generation of missions, following Europa Clipper and Mars Sample Return, to explore our solar system with e.g. a Mars Science Helicopter, a Lander for an Ocean World, and a Venus Aerobot. These future missions will require significantly higher computing power, both for Terrain Relative Navigation (during EDL and helicopter flight), and for more autonomous science data processing onboard. Radiation-hardened hardware for space applications and with high computational capability is not available in the near-term. This proposal provides a near-term solution that leverages multiple non-radiation hardened COTS processors and a middleware layer to achieve the needed reliability, availability, and fault tolerance, as part of fault detection, isolation, and recovery (FDIR). Moreover, since this design can adapt to any choice of high-performance co-processors, it provides the first and only way we know of, whereby flagship spacecraft avionics can keep up with the state-of-the-art in computer processors.



Approach and Results: The proposed architecture, using COTS high performance modules, highly-reliable RAD-hard modules, a new Interface Board, and middleware, is expected to provide flagship-class C&DH/GN&C reliability, onboard science data and autonomy processing throughput, and fault tolerance against some 2-fault scenarios. This will allow un-interrupted operation during critical mission phases, for signi-ficantly lower SWaP and cost than the state-of-the-practice.

Significance/Benefits to JPL and NASA: In the near-future, this technology can benefit the Mars Science Helicopter, and Lunar rovers needing autonomy. It will also enable # flagships with state-of-the-art computing, # highly-reliable smaller spacecraft, # improved reliability in radiatively hot environ-ments, # precision landing with hazard avoidance done by COTS co-processors, # rover autonav done by COTS co-processors, and # aerial flight on Venus, Mars, the outer planets, and Titan.

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