National Aeronautics and Space Administration

Analog to Digital Converter for a Phasemeter

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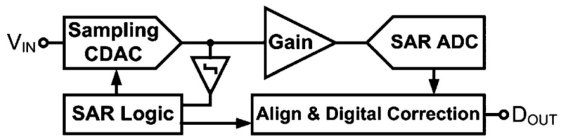
Program: FY22 SURP
Strategic Focus Area: Direct/Coherent Detectors and Arrays

Background

The objectives of this research are to develop and demonstrate a low power ADC for the JPL ASIC-based phasemeter. The phasemeter ASIC development aims at technology development for a nanometer accuracy precision laser instrument. The target ADC specification is a bandwidth of more than 50 MHz, digitized with an effective resolution of greater than 10 bits.

Approach

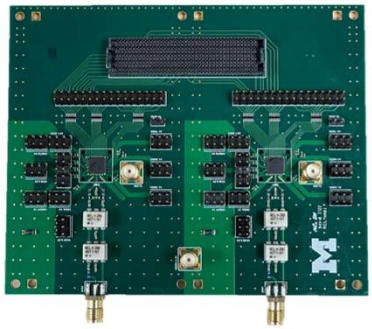


- Phasemeter performance limited by ADC
- ASIC implementation improves power efficiency
- SAR-assisted pipeline architecture is used
- This architecture offers high performance and low power
- Pipeline of SAR ADC relaxes comparator noise requirement
- Residue amplifier (RA) typically limits performance
- This work focuses on improvements to the RA

Benefits to JPL and NASA

- IP for high-resolution and low-power ADC
- Expansion of Mixed Signal ASIC PEMC task
- Dual channel design on custom substrate allows calibration tones for precision laser instrumentation

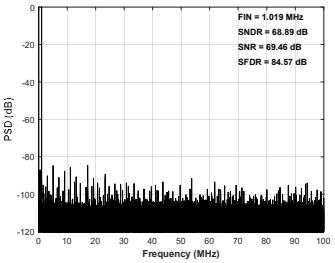
Results – Dual Channel ADC Front-end



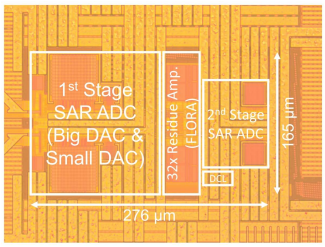
- Dual channel ADC board
- FMC connection to phasemeter testbench
- Thermal matching capability
- Independent reference clock capability

Results - ADC

- ADC fabricated in 28-nm CMOS technology
- Each ADC consumes 2.7mW from a 1.1V supply when operating at 200MS/s
- Measured SNDR for 1 MHz input signal is 68.9 dB, approx. 11 bit ENOB



SNDR performance of ADC



Fabricated chip micrograph

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Clearance Number: CL#
Poster Number: RPC#065

Publications:

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