National Aeronautics and Space Administration

Direct Back-End Integration of III-V Single Crystalline Materials in CMOS via Growth for Active Integrated Photonic Components and 3-D Integrated Sensing Technologies

Principal Investigator: Harold Greer (389); Co-Investigators: Sarath Gunapala (389), Alexander Soibel (389), Daniel Masters (791), Jun Tao (USC), Hyun Uk Chae (USC), Rehan Kapadia (USC)

Program: FY22 SURP
Strategic Focus Area: Electronics, Devices and Sensors

Objectives:

Our objective for this program was to continue to develop our III-V growth technology to demonstrate high quality III-V's on non-traditional substrates that could substantially reduce cost, simplify integration, and improve overall performance. As part of this work, we have studied the growth of InP, InAs, and InGaAs on completely non-epitaxial substrates, the growth of InP on Si substrates, and the smoothing of III-V layers using ALE. Our overarching goal is to develop a fundamental understanding of how this growth approach works and then utilize these materials for detectors, sensors and integrated photonic devices.

Background :

Moore's law is coming to an end. As improving performance by shrinking the size of transistors is no longer available, improving the functionality of computing devices will be achieved through the ability to build 3-D chips and functional diversification. However, the only feasible method of carrying this out presently is by stacking multiple computer chips together and interfacing them, which only provides modest performance improvements. The ideal approach would be direct growth of the desired high-quality semiconductor on a silicon chip. This could then be repeated until the desired 3-D systems are built. However, this is presently impossible, as all state-of-the-art semiconductor growth techniques require a large area single-crystalline substrate, such as a silicon wafer. In a real 3-D computer chip, other than the initial silicon devices, all the other devices must be grown at temperatures below 400 ^{o}C and on amorphous materials such as oxides, which are not single crystalline.

Recently, Prof. Kapadia's group has demonstrated (through work partly funded by JPL) that thin-film format crystals of InP and InAs can be grown directly on non-epitaxial surfaces such as SiO_2, Si_3N_4, graphene, W, Mo, and others at temperatures down to 200 ^{o}C. This offers a new route towards the growth of *high-performance* III-V devices directly on a Si wafer without damaging the underlying Si CMOS ROIC circuitry. By using our growth technique to first grow a crystalline III-V template on a silicon or amorphous substrate, we can create high-quality virtual substrates on which to carry out epitaxy using the well-established growth technology of MOCVD. Presently, we are exploring the use of this mixed growth approach to enable InGaAs SWIR detectors on Si ROICs via direct growth.

Approach and Results:

The most significant discovery/development over the past year was related to growth of high quality III-V's directly on Si substrates. While previous developments have focused on the growth of III-V crystals on non-epitaxial substrates such as Mo, W, SiO_2 and Si_3N_4. However, one challenge with growth on non-epitaxial substrates was that while each mesa was single crystalline, the relative orientation between mesas would vary. However, we have recently found that this approach can be used to directly grow entirely single crystalline, low defect density, mesas directly on Si. Figure 1 shows the cartoon schematic of the approach. We first take a silicon 100 wafer and use MOCVD to grow a continuous layer of InP. This layer is highly defective due to the large lattice mismatch between InP and Si. Next, we carry out TLP growth on the Si/InP substrate. This involves the deposition of patterned indium and silicon oxide mesas, followed by heating and exposure to PH_3 gas. This transforms the indium mesas to InP.

Figure 2a shows a plan view SEM image of a TLP InP mesa on the Si/MOCVD InP substrate. TEM images of the junction between TLP InP, MOCVD InP, and unreacted indium is shown in Figure 2b,c. We see that the TLP/MOCVD interface appears to filter out defects. To get a broader view of this phenomenon, we have done scanning TEM inspection of three different MOCVD/TLP growth cases. Figure 2d shows the undoped case, where only indium is present in the TLP mesa. We see that despite there being a large density of visible defects in the MOCVD InP layer, these do not penetrate into the TLP layer. Figure 2e shows the results with tin doping, where and indium/tin mesa was created and then phosphorized. This behaves similarly to the undoped case. Finally, inserting a thin tin oxide layer between the indium and MOCVD InP results in an interesting case where underlying defects do not penetrate into the growing TLP InP, however there are a number of twinning defects that are formed during TLP growth. Figure 3 shows transmission Kikuchi diffraction maps (TKD), which give 3-D crystallographic orientation maps. What we see is that the TLP InP is fully oriented with the underlying Si, with the exception of two minor twinned regions. ***This data shows that the TLP/MOCVD interface behaves as a highly efficient defect filter while still maintaining crystallographic orientation*.**

Figure 4a shows the steady state photoluminescence spectra of the underlying MOVCD InP and grown TLP InP. We observe a ~100x increase in emitted photons, illustrating that the grown material is considerably higher optoelectronic quality than the substrate on which it was grown. This is electronic data which corroborates the structural data.

Significance/Benefits to JPL and NASA:

These recent developments pave the way for growth of science grade APS IR sensors FPAs would revolutionize the design and development of IR instruments and even world class IR missions such as ROMAN and Euclid. This is potentially enabled by the approach being developed here. For the long term, developing this technology would provide JPL with a strong base that could prove revolutionary for multiple electronic and photonic devices, circuits and systems. However, beyond this return, the addition of III-V on Silicon Integrated Photonics capabilities, and multi-modal sensing capabilities would be enabling for a broad variety of programs at JPL.

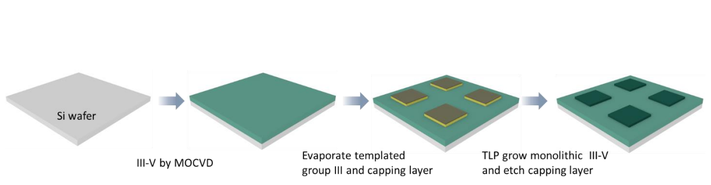

Figure 1. Schematic of heteroepitaxial approach to growth of III-V's on silicon using TLP

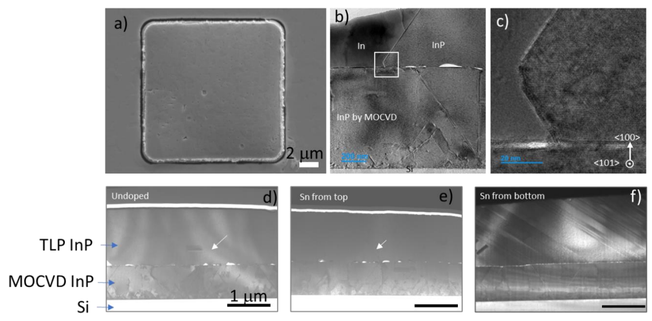

Figure 2. a) SEM of TLP InP on MOCVD InP/Si substrate. b) TEM of triple interface between MOCVD InP, TLP InP, and unreacted indium. c) Higher magnification view of triple interface. d) STEM view of Si/MOCVD InP/TLP InP stack showing defects being filtered at the MOCVD/TLP interface. e) STEM of Sn doped TLP InP. f) STEM of Sn doped TLP InP when an interfacial layer is introduced between the MOCVD and TLP layers.

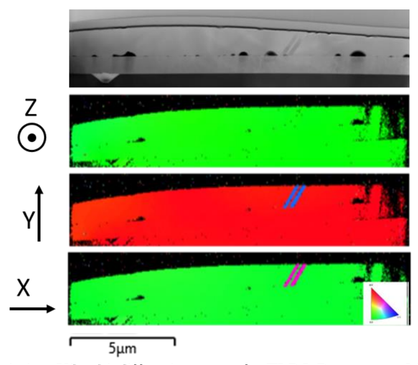

Figure 3. a) Transmission Kikuchi diffraction maps for TLP InP grown on MOCVD InP. Top figure is a cross sectional SEM, and the bottom three figures are the x, y, and z orientations of the grown TLP InP, MOCVD InP, and Si. The complete matching shows that the grown InP is oriented in all three axes.

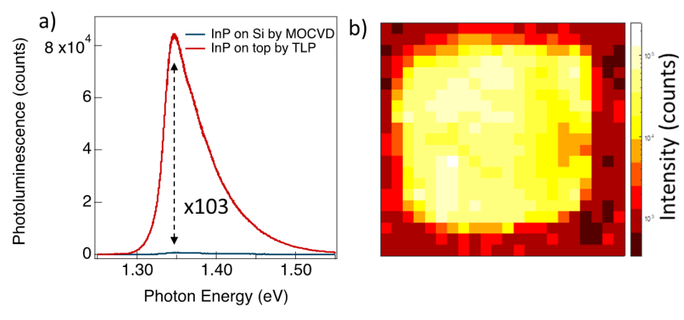

Figure 4. a) Steady state photoluminescence spectra of the TLP InP and the underlying MOCVD InP. b) PL intensity map of a TLP InP mesa (bright PL) on the MOCVD InP/Si substrate (dimmer PL).

National Aeronautics and Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

www.nasa.gov

Publications:

(one in preparation – "Liquid Phase growth of III-V on Silicon for highly efficient defect filtering)

PI/Task Mgr. Contact Information:

Email: Frank.Greer@jpl.nasa.gov

Clearance Number: CL#
Poster Number: RPC#