National Aeronautics and Space Administration

A CMOS-Molecular-Clock Integrated Platform for Deep Space Communications, Navigations and Radio Science

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Program: FY22 SURP
Strategic Focus Area: Electronics, Devices and Sensors

Objectives:

The objective of this work is to investigate and experimentally demonstrate a few key technologies towards a monolithic molecular clock integrated chip with ultra-low power and cost. Such a clock can be used to provide long-term stability calibration of temperature-compensated crystal oscillators (TCXOs), which are widely deployed in aerospace communication and sensing instruments. The monolithic molecular clock chip can improve the long-term (>100s) stability of TCXO by 10-100 times, with 0.1 cm3 added volume. We expect this JPL-MIT collaborative partnership to infuse molecule-based quantum frequency/timing technology and terahertz semiconductor technology for future NASA science and exploratory missions.The second year sub-objective is to design a highly efficient RF to sub-terahertz generation chip to enable future chip-scale molecular clocks.

Background:

The concept of a chip-scale molecular clock was conceived by Han's group and later experimentally demonstrated using a standard 65nm CMOS chip and a metal single-mode THz waveguide gas cell [1,2]. By using a CMOS spectrometer to probe the transition frequency of the rotational mode of carbonyl sulfide (OCS) molecules in the low-THz (i.e. 0.1~1THz, 0.23THz in [1,2]) regime, the chip-scale molecular clock offers a time-keeping solution with small size, power, weight, and cost (SWaP-C). TCXOs are the gold standard in most space-borne communications systems in NASA missions. Space qualified Chip Scale Atomic Clocks (S-CSAC) from Microsemi Corp. provide 3x10^-11 stability at 100s integration time with a volume of 16 cm3. In this proposal, key technologies towards a new, highly miniaturized molecular clock chip will be developed. Such a chip will be used to calibrate the frequency of a TCXO at a comparable stability with S-CSAC but with only 0.1 cm3 addition of volume.

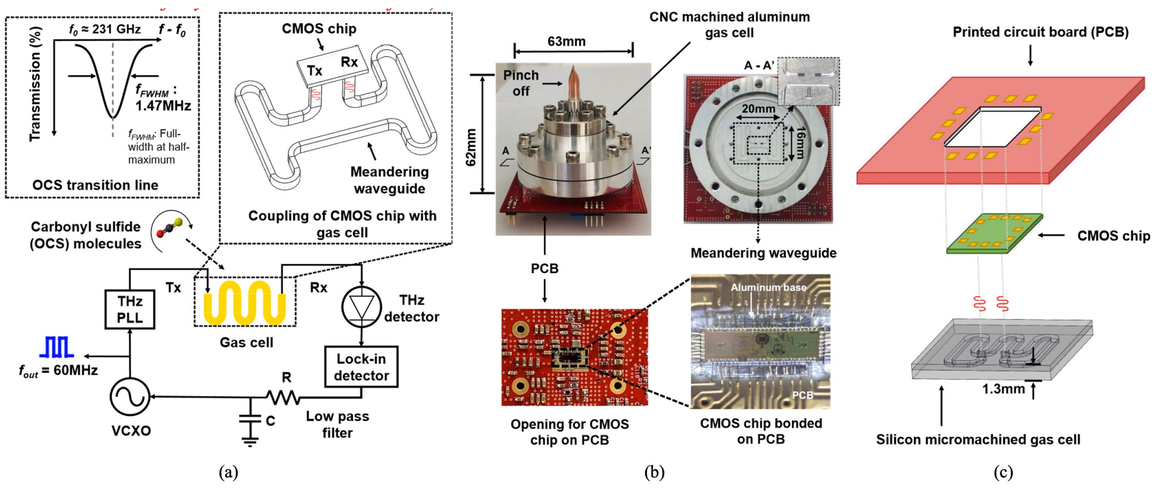
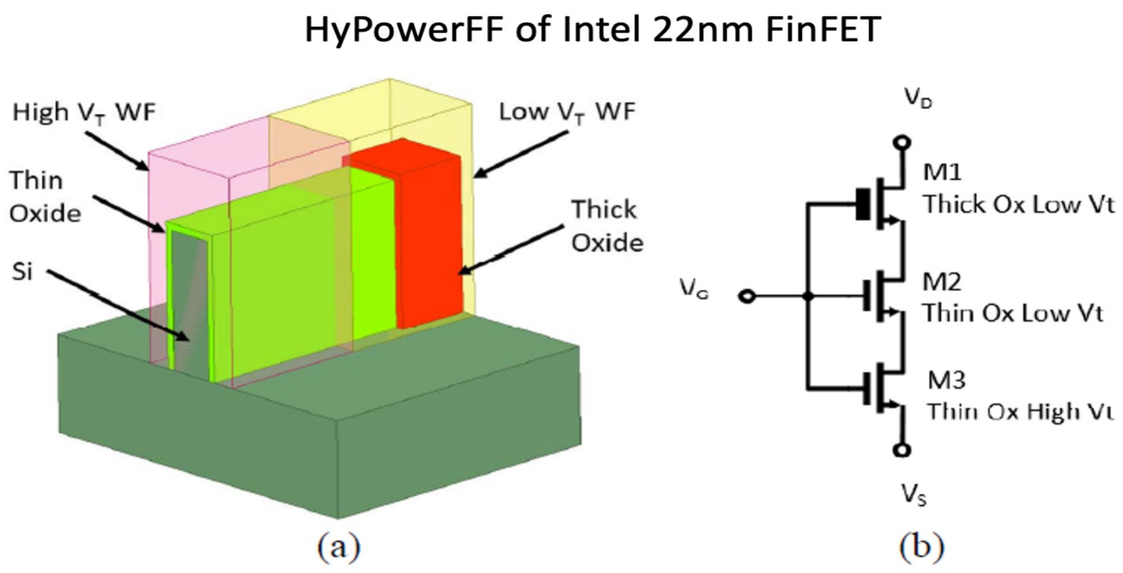


Figure 1. (a) Simplified schematic of the chip-scale molecular clock (CSMC). (b) The previous implementation of CNC machined aluminum gas cell using pinch-off sealing with a volume of ~246 cm3 [3]. (c) Proposed 3D stack using silicon micromachined gas cell



(c)

Device	Peak $g_m \times R_{out}$	Peak f_T	Peak f_{max}	$V_{Breakdown}$
120nm HyPowerFF	148	75GHz	290GHz	6.3V
160nm HyPowerFF	160	55GHz	260GHz	7.1V

Figure 2. (a) HyPowerFF device structure; (b) equivalent model [Intel, IMS2020]; (c) Performance summary of HyPowerFF

Approach and Results:

The OCS gas was traditionally sealed inside of a CNC-machined aluminum waveguide using pinch-off sealing (Fig. 1b), leading to a large volume of ~246 cm3, high cost, and unscalable manufacturing. Silicon micromachining is an attractive option for the above goal, as it is common for gases to be sealed inside cavities during wafer bonding. This enables an "all-silicon" clock assembly depicted in Fig. 1c, where the CMOS chip is stacked on top of the gas cell waveguide, introducing a unique need for a pair of waveguide bends to couple to the CMOS chip.

Figure 2 shows that we have the access to a high speed and high power transistor in Intel 22nm FinFET. Its breakdown voltage can go up to 6.3V with a peak fmax of 290 GHz. Figure 3 shows the simulated results of a common-source amplifier based on the mentioned high power transistor. Its saturated output power can achieve 19.6 dBm@130 GHz with a gain of 4dB and a PAE of 9.15%. Figure 4 shows that we proposed a modified PA core topology based on MRR (multilayer ring resonator) embedded in the traditional peak-gain theory PA core. It can create multiple resonances to achieve broadband matching. Figure 4 also shows that we proposed to use a neutralization capacitor to firstly eliminate the Cgd of the transistor in a peak-gain theory PA core to further increase the Gmax bandwidth. Figure 5 shows the design and the simulated results of the SIW amplifier collaborating with Cornell.

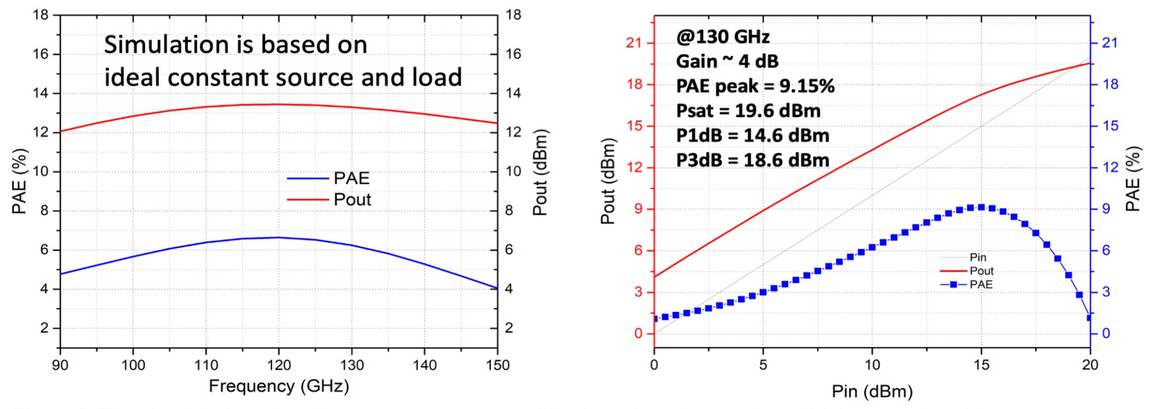


Figure 3. The simulated results of a common-source amplifier based on the mentioned high power transistor

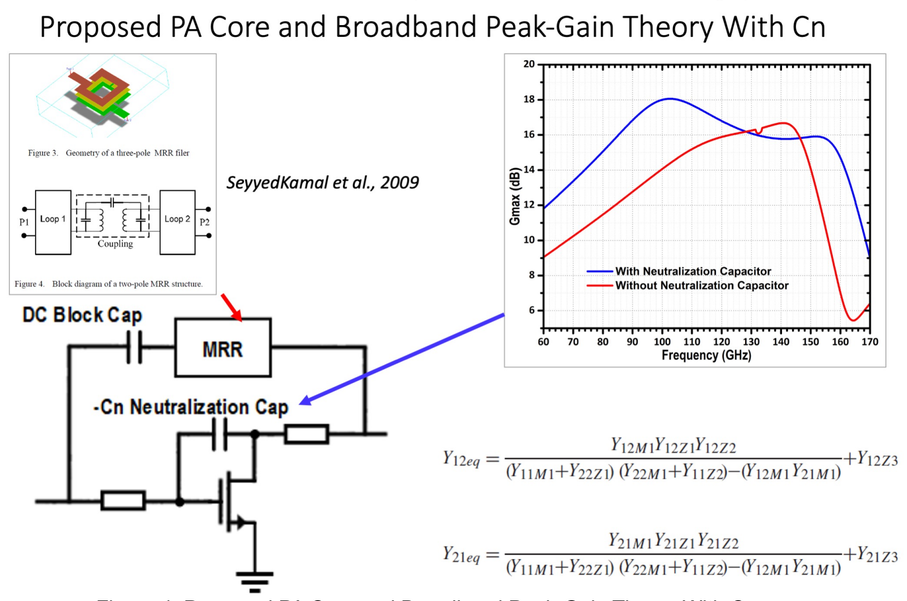


Figure 4. Proposed PA Core and Broadband Peak-Gain Theory With Cn.

Significance to NASA/JPL:

In the 2nd year's effort, we have been focusing on the high efficient sub-terahertz generation technology for the molecular clock. The chip fabrication process depends critically on the "pre-fab" design and simulations. Sub-terahertz signal generation is the largest contributor in the power consumption in the chip-scale molecular clock. These are important steps to infusion low power technology into the "wafer clock" concept we envisioned.

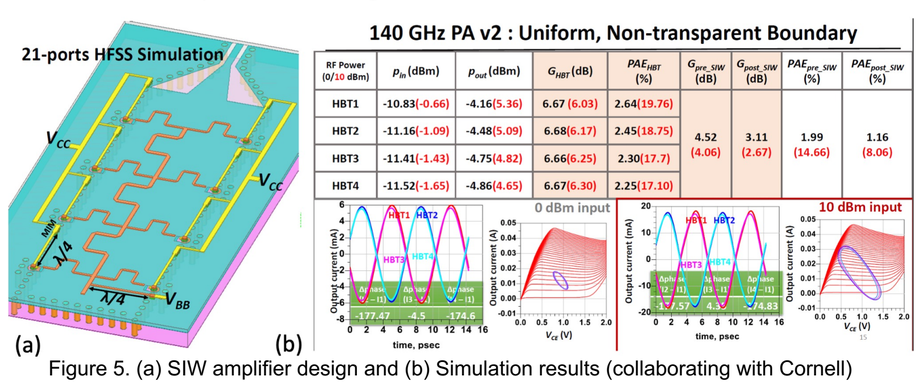


Figure 5. (a) SIW amplifier design and (b) Simulation results (collaborating with Cornell)

References:

[1] C. Wang, X. Yi, J. Mawdsley, *et al.*, "An on-chip fully electronic molecular clock based on sub-terahertz rotational spectroscopy," *Nature Electronics*, vol. 1, no. 7, pp. 421–427, 2018.

[2]"Chip-Scale Molecular Clock," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 914–926, 2019.

[3] C. Wang, *et al.*, *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 566–580, 2021.

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Publications:

[A] Alec Yen et al., "Integrable timing on silicon wafer supporting CubeSats-based Communications, Navigation and Radio Science", AIAA ASCEND 2022, accepted as an oral presentation

[B] Kim, Mina, et al. "A Sub-THz CMOS Molecular Clock with 20 ppt Stability at 10,000 s Based on Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration." 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). IEEE, 2022.

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