National Aeronautics and Space Administration

FY23 Strategic Initiatives Research and Technology Development (SRTD)

Cell Library Assurance for Strong ASICs (Class A)

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Strategic Focus Area: Cell Library Assurance for Strong ASICs (Class A) | **Strategic Initiative Leader:** Harald Schone

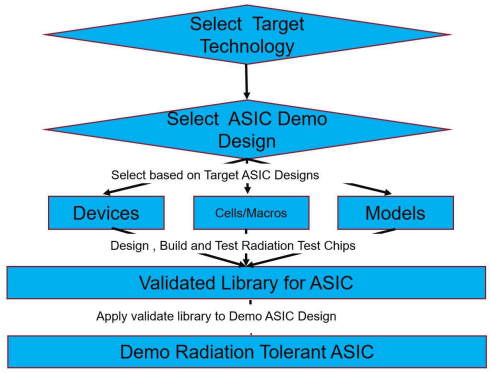
Objectives

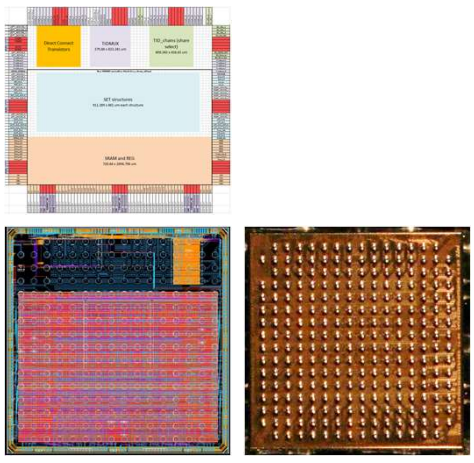
Develop an **upfront assurance approach** that aims to enable JPL to design and fabricate reliable, radiation tolerant ASICs capable of supporting the bulk of our missions by :

Removing two key factors hindering JPL ASIC implementation in the past 1) specialized cell libraries (radiation hardened cell libraries) 2) in-depth radiation design expertise.

Develop and validate instead

1) Automotive grade library with high reliability of 15-years and high level of process control
2) advanced modern technology
3) an efficient radiation test matrix for the automotive cell library over a series of test chips
4) identifying the preferred library elements in design for radiation guidelines
5) validate potential for first run success in sample design





From the top-left, clockwise:
1. Floorplan of the JPL demonstration ASIC.
2. Picture of the fabricated and bumped ASIC
3.. The layout of the ASIC

Background

- Over the last 35 years, we saw miniaturization and automation transforming all aspects of our every day lives with the arrival of cell phones with powerful computing and communication in our hands and smart appliances to handle operations from ordering groceries to water the plants in our homes .
- Such miniaturization and automation (autonomy) represent how advances in electronics can powerfully transform our space systems, but the commercial electronics underlying commercial miniaturization and automation do not have sufficient reliability and space environmental tolerance to be directly inserted into our systems.
- Our missions are still primarily relying on dated but reliable and space tolerant military grade electronics. The performance gap between the two types of electronics is already orders of magnitude and still growing.
- We have to find ways to harness the power of modern electronics & bridge that gap.

Approach and Results

Owing to their tailor-made designs, ASICs can offer significant advantages over commercially available microelectronics in the areas of size, weight, and power (SWaP). However, ASIC development poses several non-trivial difficulties and– while often desired by projects– it is currently seen as an impractical option. **Those difficulties in mind, our intent with this initiative is to refine the ASIC design flow within JPL to something as straight forward as the FPGA design flow, such that missions may have a direct path towards ASIC development and utilization.**

For the ASIC fabrication, we have strategically chosen the Global Foundries automotive fabrication technology (22FDX) for its many benefits.

1) The GF 22nm production line is one of the highest volume lines in the global market, guaranteeing the highest yielding, stable production to support the 10+ year product run requirement of the automotive industry.
2) The technology is offered on silicon-on insulator (SOI) substrate known to be impervious to single event latchup. This characteristic vastly mitigates the most vexing problem in the use of COTS products.
3) The total ionization dose (TID) capability of this 22nm line is known to be significantly higher than 100 krad(Si), sufficient for most of NASA's missions.
4) 22nm technology node provides high speed devices and I/Os to support advanced logic functions for future computational requirements while at the same time mature enough to support the range of mixed signal and RF functions that are also key to spacecraft electronics miniaturization.
5)Monthly shuttles available creates reliable development and design scheduling.

In FY20, pathfinder test chip was designed and built.

In FY21& FY22 a second test chip was built, with circuits to quantify heavy ion, laser and ion dose effects

1) Over 100 structures designed to cover transistor voltage and sizes.
2) Both digital and analog design flows being exercised.
3) Fully validated input output circuit ring, addressing the weakness of test chip 1.
4) The packaging substrate supports high frequency testing appropriate for 22FDX.

In FY23 we completed TID and Initial TID testing of the test structures to generate data for cell selection and radiation modeling

1) low voltage transistor TID testing with TID MUX test structure
2) SEE testing on SRAMs and Register files.

In FY23 we completed design and fabrication on a JPL demonstration ASIC utilizing a JPL flight memory controller FPGA design to validate our methodology base on the learning from the test chipsWe have developed and demonstrated a methodology for effective radiation-tolerant ASIC design to support future NASA/JPL missions based on an upfront assurance method utilizing cell selection and design for radiation guidelines on the 22nm GF process technology. Through the execution of a series of 3 test chips, we learned to utilize the design and foundry tools, generated quantitative radiation characterization for various radiation effects, and set up environments for radiation modeling. We have demonstrated radiation-aware design and cell selection methods as well as modeling of baseline radiation performance by completing new ASIC design based on a JPL FPGA memory controller design from the MARS projects. This design has completed fabrication, but unfortunately the task did not receive enough funding to complete the package and test of the chip. However, the knowledge gained and the engineering tools developed from this task will support future NASA/JPL ASIC designs to a significantly higher first pass success rate, especially for the effective and efficient conversion of FPGA designs to advance node ASICS for flight projects.

Significance/Benefits to JPL and NASA

We have developed and demonstrated a methodology for effective radiation-tolerant ASIC design to support future NASA/JPL missions based on an upfront assurance method utilizing cell selection and design for radiation guidelines on the 22nm GF process technology. We have demonstrated radiation-aware design and cell selection methods as well as modeling of baseline radiation performance by completing new ASIC design based on a JPL FPGA memory controller design from the MARS projects. The knowledge gained and the engineering tools developed from this task will support future NASA/JPL ASIC designs to a significantly higher first pass success rate, especially for the effective and efficient conversion of FPGA designs to advance node ASICS for flight projects.

Publications:

[A] L. T. Clark et al., "A Transistor Array for Extracting Total Ionizing Dose Threshold Voltage Shifts," 2022 IEEE International Integrated Reliability Workshop (IIRW), South Lake Tahoe, CA, USA, 2022, pp. 1-4, doi: 10.1109/IIRW56459.2022.10032746..
[B] R. Melendez, L. Martinez, L. T. Clark, C. S. YoungScioritino, S. M. Guertin and J. Yang-Scharlotta, "Consistent and Repeatable Transistor Level TID Transistor Array Measurement," 2023 IEEE Radiation Effects Data Workshop (REDW) (in conjunction with 2023 NSREC), Kansas City, MO, USA, 2023, pp. 1-4, doi: 10.1109/REDW61050.2023.10265838.
[C] R. M. Melendez, S. M. Guertin, J. Yang-Scharlotta and L. Clark, "SEE Test Results for SRAM and Register Files Compiled on 22nm Fully-Depleted-Silicon-on-Insulator (22FDX)," 2023 IEEE Radiation Effects Data Workshop (REDW) (in conjunction with 2023 NSREC), Kansas City, MO, USA, 2023, pp. 1-3, doi: 10.1109/REDW61050.2023.10265855

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