National Aeronautics and Space Administration

FY23 Topic Areas Research and Technology Development (TRTD)

On-chip Power-combining Networks with Integrated Harmonic Terminations for Highly-efficient, High-power SSPAs

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Strategic Focus Area: RF and Optical Communications

Objectives

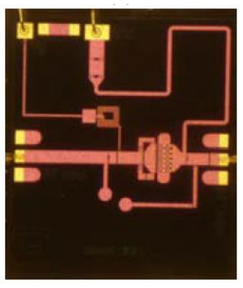
- Demonstrate a design method which provides a solution to simultaneously improving efficiency and output power of microwave MMIC SSPAs
- X/Ka-band characterization of new-gen GaN transistors for JPL/NASA applications
- Design an X-band (FY'21)and Ka-band (FY'22) GaN MMIC

Problem Description

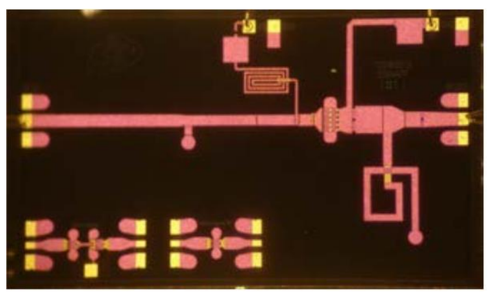
SSPAs are designed either to optimize output power or efficiency

- Harmonic terminations significantly improve power-added efficiency (*PAE)*
- Power-combiners significantly improve output power (P_{out})
  → **Need power-combiners with integrated harmonic terminations**
  - Technology which scales the output power of highly-efficient SSPAs

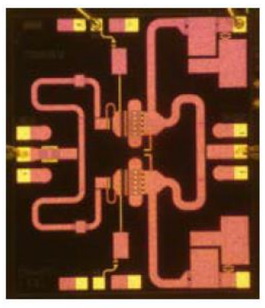
Below are three 10 GHz MMICs, designed on same GaN process [1]



Harmonic terminations: No
Power combiner: None
P_{out} = 2.5-W , *PAE* = 49%



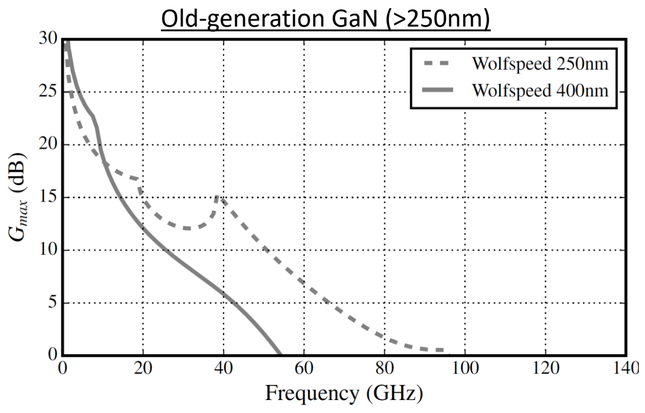
Harmonic terminations: Yes
Power combiner: None
P_{out} = 2.5-W , *PAE* = 69%



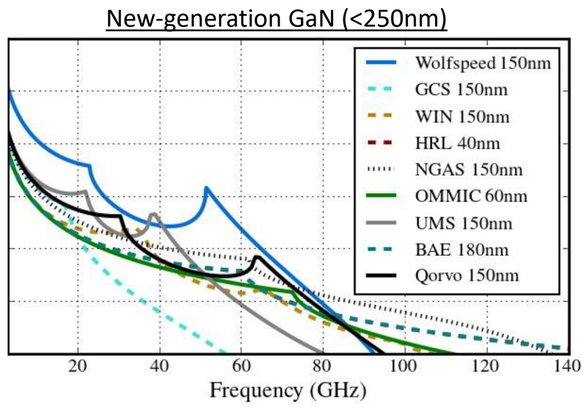
Harmonic terminations: No
Power combiner: Yes
P_{out} = 4-W, *PAE* = 48%

Background

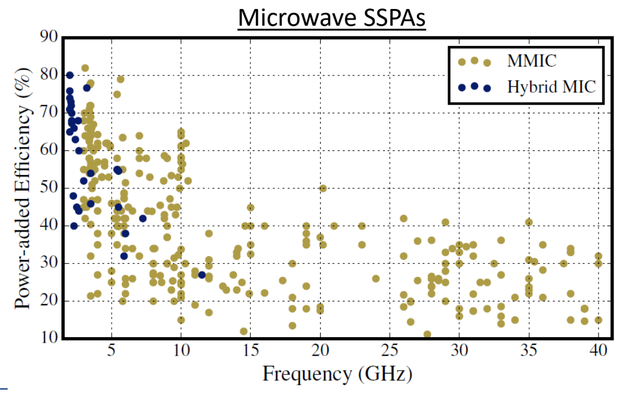
Old-generation GaN (>250nm)



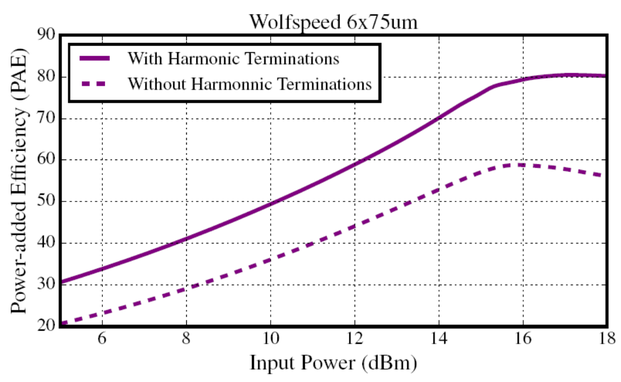
New-generation GaN (<250nm)



Microwave SSPAs

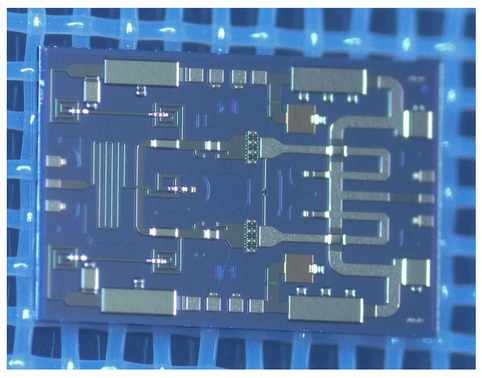


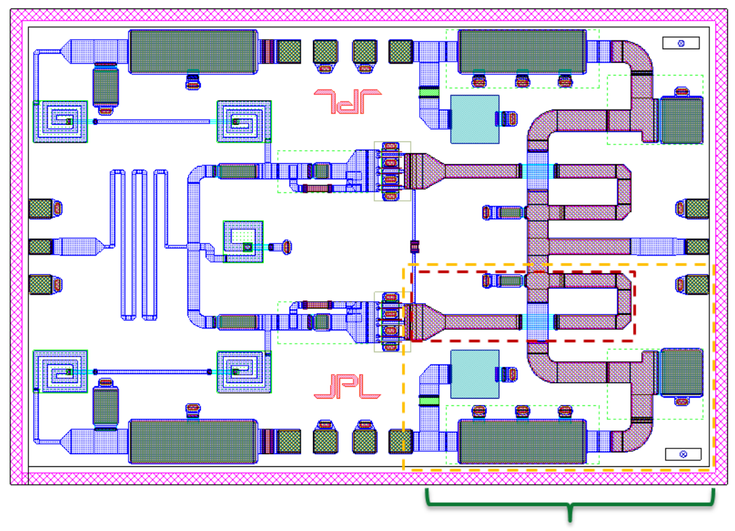
Wolfspeed 6x75um



Results

JPL GaN MMIC SSPA for DSN X-band Downlink
New-gen 150nm GaN/SiC process (Wolfspeed)
Chip Size: 3mm x 2mm (compare to λ = 35mm)
Simulated Performance: ***PAE* = 58%, P_{out} = 5 W**



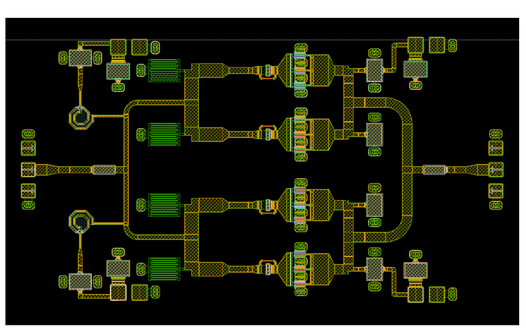


Integrated $2f_0$ Resonator
- Co-designed with Bias line
- Resonates with transistor drain-to-source capacitance to simplify f_0 matching

Bias Line co-designed with $2f_0$ resonator + f_0
- Provides >30dB DC/RF isolation
- Resonates with transistor drain-to-source capacitance to simplify f_0 matching

On-chip Power Combiner
w/ integrated harmonic terminations + f0 matching

JPL Ku-band GaN MMIC SSPA
New-gen 120nm GaN/SiC process (WIN Semiconductors)
Chip Size: 3mm x 2mm (compare to λ = 12mm)
Simulated Performance (27GHz): ***PAE* = 42%, P_{out} = 6 W**



Technique scaled to
4-way on-chip power combining
(integrated harmonic reflections)

References: [1] S. Schafer, M. Litchfield, A. Zai, Z. Popovíc, and C. Campbell, "X-band MMIC GaN power amplifiers designed for high-efficiency supply-modulated transmitters," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, Jun. 2013, pp. 1–3

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