National Aeronautics and Space Administration

Low-power giga sampling digitizer for large-format far-IR detectors

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FY23 Topic Areas Research and Technology Development (TRTD)
Strategic Focus Area: Components and Integrated Systems

Objectives: The objectives of this research are to develop and demonstrate a low-power giga sampling digitizer for the JPL ASIC-based far-infrared (far-IR) detector. The digitizer ASIC is specifically designed to be compatible with large-format arrays of microwave kinetic inductance detectors (MKIDs). We aim to develop a single digitizer ASIC capable of reading out simultaneously up to 2K pixels of detectors distributed in a frequency-multiplexed form over the 2 GHz bandwidth.
Our strategy to design a promising digitizer for successfully implementing large-format arrays of MKIDs into space-borne far-IR detectors follows three phases.

1. The first phase of this project considered the overall design requirements and the optimum digitizer architecture. This phase has been successfully completed this year.
2. The digitizer will be implemented in 65nm CMOS process in year 2. The targeted power consumption is 100mW per channel.
3. The final phase of the project will fabricate the digitizer ASIC, in which two channels are combined, and evaluate its performance.

Background: The Decadal Survey in Astronomy and Astrophysics for the 2020s suggests the implementation of “probe” class line with mission cost of ~$1.5B. The survey lists a far infrared (far-IR) imaging or spectroscopy mission as one of the two areas for the first probe competition. JPL has a plan to submit a proposal to this competition (PRIMA). The Lab developed MKIDs for far-IR and sub-mm astronomy, which are the most attractive radiation detectors as they achieve ultimate sensitivity and provide the possibility to create very large arrays, over 10K pixels, due to their intrinsic capability of frequency division multiplexing. One of the most critical bottlenecks in implementing these detectors for space-borne large-format imager is the absence of a low-power, compact readout electronics. Therefore, an ASIC implementation promises the most power-efficient and small-area solution. This research focuses on a single-chip digitizer approach that delivers high performance and is compatible with a spectrometer ASIC implementation.

APPROACH AND RESULTS

The objectives of the first phase have been accomplished by following three steps.

1. The digitizer requirements have been defined and verified using the top-level readout simulator newly developed.
2. The digitizer architecture has been finalized to meet design requirements with low power consumption.
3. The essential calibration scheme for the proposed low-power architecture has been developed and verified in a high-level simulation.

Top-level readout simulator for digitizer requirements

To accurately assess the requirement of analog-to-digital converters (ADCs) in the digitizer ASIC, we have developed an MKID readout electronics simulator in a MATLAB/Simulink environment. ADC resolution is one of the key parameters that must be investigated. The resolution reported in the previous MKID readout systems [1-2] is 10 or 12 bits. These numbers can significantly affect development efforts and hardware resources (> ~4× power and area). We have analyzed signal-and-noise propagation utilizing the simulator to decide its optimal number, including all hardware components, such as the comb generator, RF electronics, MKID arrays, and digitizer. Two simulations with different ADC performances, shown in Figure 1, have been performed. The results shown in Figure 2 reveal the resolution of 12-bit is more reasonable because it makes the ADCs not the most dominant noise contributors compared to the other components. Further investigation of higher-resolution ADCs was not necessary because 12-bit meets the requirement.

Digitizer architecture

After a thorough literature survey, we have chosen the time-interleaved successive approximation register (TI-SAR) ADC as a digitizer design scheme. The time-interleaved (TI) approach can increase the effective conversion rate of an ADC by multiplexing several ADCs in parallel. This architecture benefits power efficiency because the conversion rate can be increased linearly proportional to the number of interleaved channels. In general, the power consumption of an ADC grows much faster rather than linear. Figure 3 shows a high-level block diagram of the ADC architecture reported in [3], which will be implemented in year 2. Figure 4 summarizes the targeted performance of the ADC. Our digitizer ASIC will be targeted to have two ADCs to support the I/Q signal processing of 2K pixels of MKID arrays.

Digital calibration algorithm

The TI-SAR ADC architecture inevitably introduces error sources that represent a major bottleneck for a power-efficient design while keeping its desired performance. The errors mainly come from the capacitor mismatches, common for both the single-channel and the parallel architecture, and the timing mismatches, only present in the TI architecture. To investigate the effects of these error sources, a behavioral model of the TI-SAR ADC has been implemented utilizing the modeling technique proposed in [4]. The mismatches must be calibrated to avoid performance degradation of the ADC. A digital calibration has been developed using the behavioral model based on the least-mean-square (LMS) algorithm proposed in [3]. We have verified that the algorithm can calibrate the capacitor mismatches in all individual ADC channels and the inter-channel gain and timing mismatches (Figure 5). This means the errors introduced in this power-efficient architecture can be sufficiently calibrated to meet target requirements.

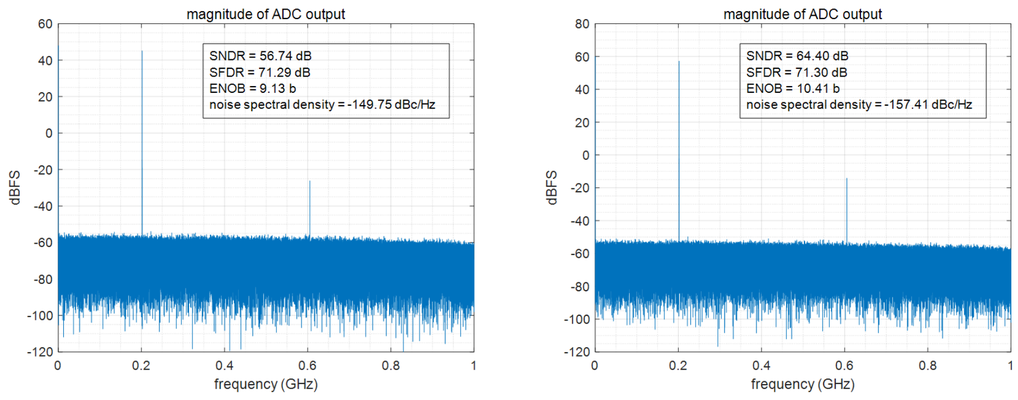

Figure 1. Spectrum of the two different ADCs used in the top-level simulation to decide an optimum number of resolutions between 10-bit (Left) and 12-bit (Right).

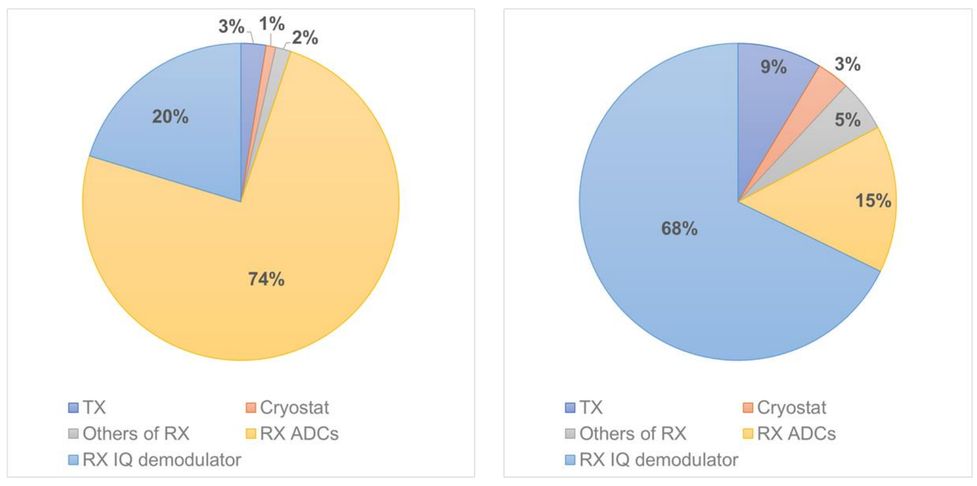

Figure 2. Simulation results of noise contribution breakdown with the two different ADCs having 10-bit (Left) and 12-bit (Right) resolutions, respectively.

Significance: The final goal is a single-chip solution for commissioning the large-format (> 25k MKIDs) far-IR detectors into the flight missions listed in the Decadal Survey in Astronomy and Astrophysics for the 2020s. Through this Topical RTD, the digitizer will be developed. At the same time, the comb generator design will be implemented with the support of the proposal entitled “CMOS integrated comb generator for a large format MKID array,” selected by the ROSES Astrophysics Research and Analysis (APRA) program in 2022. Both research and development will closely collaborate with the Microdevices Laboratory at JPL to make ASICs compatible with JPL’s MKID arrays. Our ultimate goal is to combine a comb generator and a digitizer into a single-chip solution and integrate it into PRIMA.

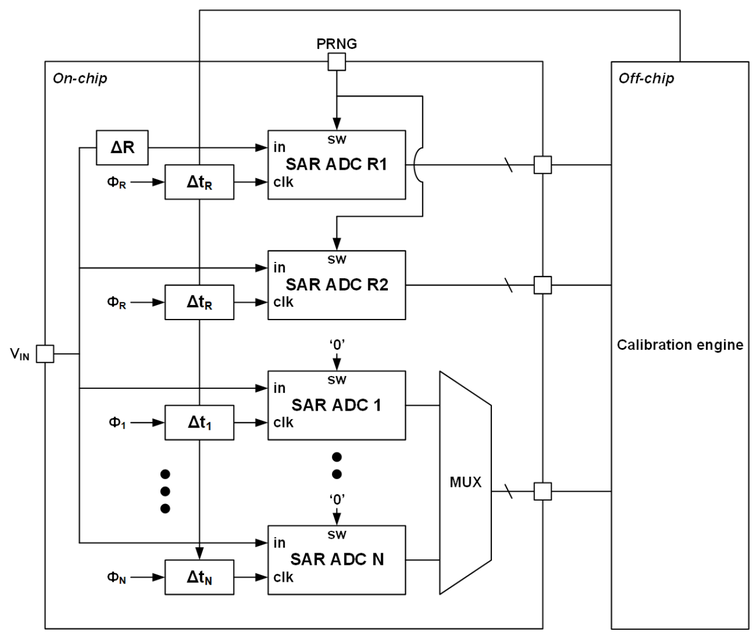

Figure 3. High-level block diagram of the single-channel TI-SAR ADC architecture.

Architecture	TI-SAR ADC
Technology	65 nm
Supply voltage	≤ 1 V
Sampling rate	2 GS/s
Resolution	12-bit
Power	100 mW per channel

Figure 4. ADC performance summary

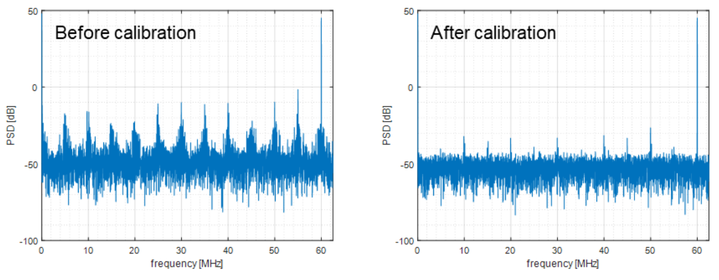

Figure 5. Spectrum before (Left) and after (Right) calibration of a single SAR ADC with a sampling rate of 125 MS/s. The digital calibration helps SNDR performance increase by a factor of 13 dB. 16 SAR ADCs will be interleaved to operate in 2 GS/s while channel-to-channel mismatch is also calibrated.

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