National Aeronautics and Space Administration

FY23 Strategic University Research Partnership (SURP)

A CMOS-Molecular-Clock Integrated Platform for Deep Space Communications, Navigations and Radio Science

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OBJECTIVES

The objective of this work is to investigate and experimentally demonstrate a few key technologies towards a monolithic molecular clock integrated chip with ultra-low power and cost. We expect this JPL-MIT collaborative partnership to infuse molecule-based quantum frequency/timing technology and terahertz semiconductor technology for future NASA science and exploratory missions. The third-year sub-objective is to implement a highly efficient RF-to-terahertz generation chip to enable future chip-scale molecular clocks, following the 2nd year's design work.

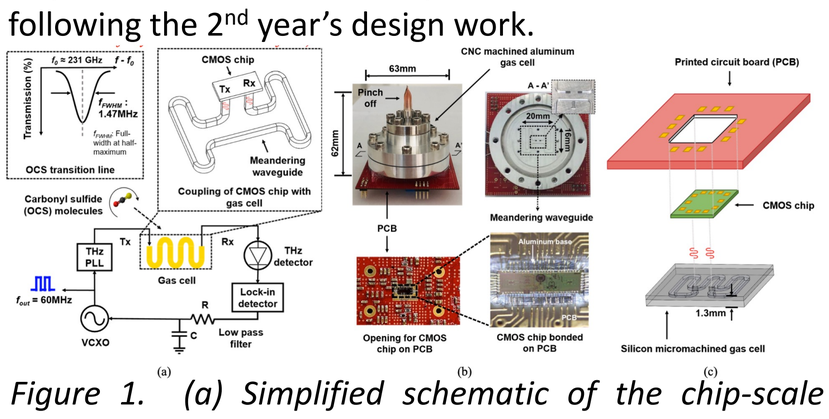

Figure 1. (a) Simplified schematic of the chip-scale molecular clock (CSMC). (b) The previous implementation of CNC machined aluminum gas cell using pinch-off sealing with a volume of ~246 cm3 [3]. (c) Future 3D stack using silicon micromachined gas cell

BACKGROUND

The concept of a chip-scale molecular clock was conceived by Han's group and later experimentally demonstrated using a standard 65nm CMOS chip and a metal single-mode THz waveguide gas cell [1,2]. By using a CMOS spectrometer to probe the transition frequency of the rotational mode of carbonyl sulfide (OCS) molecules in the low-THz (i.e. 0.1~1THz, 0.23THz in [1,2]) regime, the chip-scale molecular clock offers a time-keeping solution with small size, power, weight, and cost (SWaP-C). TCXOs are the gold standard in most space-borne communications systems in NASA missions. Space-qualified Chip Scale Atomic Clocks (S-CSAC) from Microsemi Corp. provide 3x10^-11 stability at 100s integration time with a volume of 16 cm3. In this proposal, key technologies towards a new, highly miniaturized molecular clock chip will be developed. Such a chip will be used to calibrate the frequency of a TCXO at a comparable stability with S-CSAC but with only 0.1 cm3 addition of volume. The leading power consumption element in the molecular clock is the THz source. Currently, the burgeoning interest in CMOS-based compact THz sources stems from their small form factor, high scalability, and compatibility with digital systems. However, the operating frequency of THz sources generally approaches or even exceeds the f_{max} of CMOS transistors, resulting in limited power gain. The 3rd year effort was focused on resolving this issue.

	This Work*	ISSCC 2022	MWCL 2022	TMTT 2020	IMS 2021
Technology	22nm CMOS	65nm CMOS	130nm SiGe	130nm SiGe	130nm SiGe
BW freq	224-290	134-148	205-273	223-350	212-260
FBW	25.7%	10%	17%	44.3%	20.3%
TX Power (dBm)	23.8	11.2	6.2	2.3	5.5
Radiated Power (dBm)	20.8	6.2	N/A	N/A	N/A
DC Power (mW)	10930	405	429	537	270
Die Area (mm^2)	12	3.1	0.58	1	0.29

*Simulated results. 2x15 ways

Figure 5, Performance comparison with prior effort.

SIGNIFICANCE OF RESULTS/BENEFITS TO NASA/JPL

The research effort in the 3rd year partially demonstrated the feasibility of using the CMOS technology to generate a high-power THz signal to probe the molecular lines in the frequency range from 220-300GHz. The availability of this level of power enables the JPL-MIT team to design future molecular clocks for a wide range of applications considering different sizes, weights, and power. For example, the potentially achievable 20dBm power at ~ 230GHz allows a significantly higher performance of the molecular clock using non-on-chip and/or non-waveguiding gas cells using a variety of different materials such as quartz and sapphires. The high power also allows a massive waveguiding topology on-chip for an innovative approach in molecular spectroscopy. This work allows a strong position for the JPL-MIT team for competitive proposals to NASA and DoD agencies to apply the molecular clock technology to different mission needs.

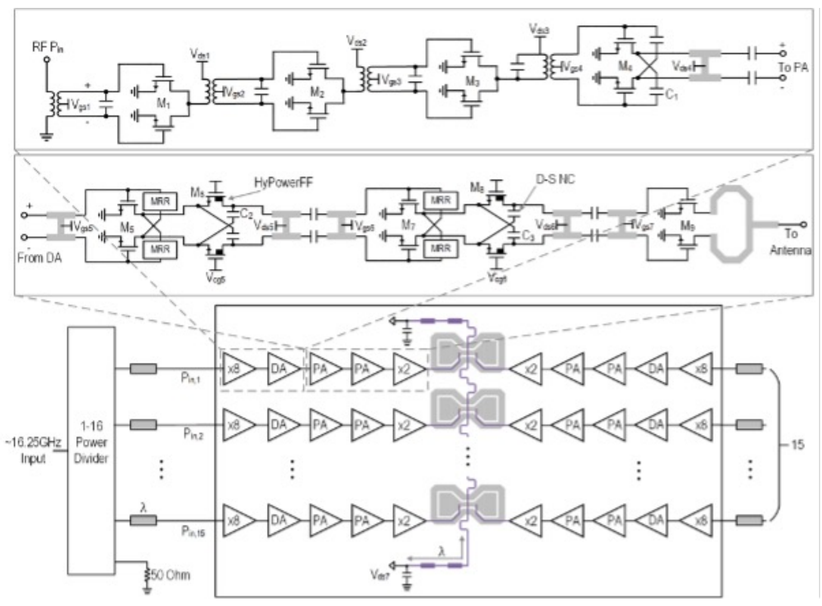

Figure 2. System diagram and circuit schematic of the proposed THz source chip.

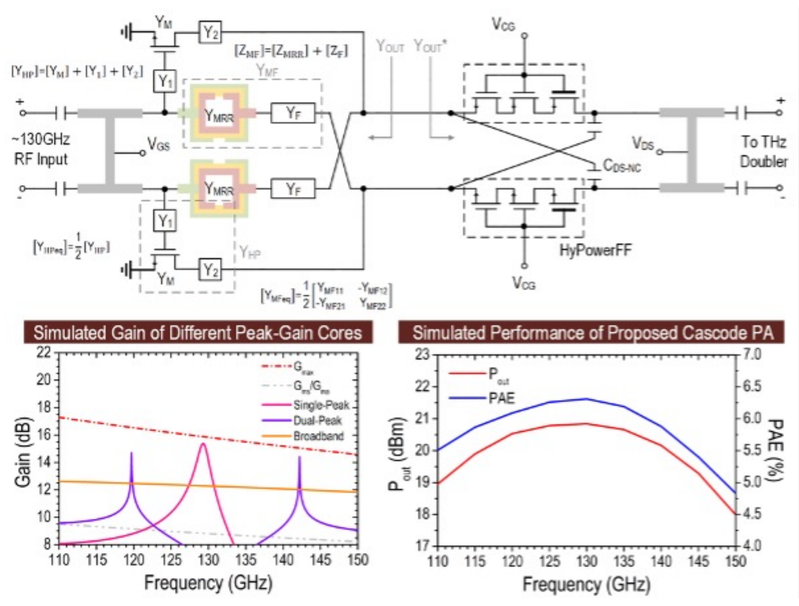

Figure 3. Schematic and analysis of the proposed cascade PA, simulated maximum available gain of different types of peak-gain cores (single-stage common source differential amplifier), and simulated output power and PAE of the cascade PA versus frequency.

APPROACH AND RESULTS

To address the power limitation issue, the peak-gain-core theory has been used to realize the maximum achievable gain (G_{max}) based on embedding networks, which is approximately four times greater than the unilateral power gain (U). The traditional peak-gain-core theory is narrowband. The frequency-dependent inductance characteristics of the transmission line were employed to implement the dual-peak-gain-core technique to realize the broadband G_{max} considering the load and impedance matching [4], while the gain between two peak-gain frequencies drops. Another method for increasing radiated power is to employ high-efficiency backside radiation. To mitigate losses attributed to silicon, a silicon lens has been affixed to the rear of the chip [5]. Alternatively, high radiated power can be attained by incorporating a large on-chip array [6] or employing multiple chips. However, the use of bulky and expensive silicon lenses imposes limitations on the scalability of antenna arrays and presents challenges in terms of thermal management.

Figure. 2 shows the fifteen 2-way amplifier-multiplier-chain cells that are used to generate a ~130GHz THz signal, which is subsequently doubled by a THz doubler and radiated by a broadband bowtie-shape slotline antenna array. The topology of PA is depicted in Figure. 3. A pair of high-performance (HP) NMOS transistor arrays is employed for common source amplification including the consideration of the designs used in [7][8]. The simulated maximum available gain of the proposed broadband peak-gain core is in comparison to other types of peak-gain cores. An ultra-high one-way output power of 20.8dBm is achieved at 130GHz with a DC voltage of 5V, and the PAE exceeds 4.8% over the frequency range from 110GHz to 150GHz.

Figure 4 shows the photo of the fabricated chip and the PCB for the chip testing and performance demonstration. The simulated thermal performance using Ansys Icepak is presented in Figure 4. The simulated maximum chip temperature is 68.965 °C. Due to the flip-chip bonding infrastructure issue at MIT, the measurement is undergoing during this report being prepared, and we are not able to show the measured results in this report. Instead, we showed the simulated result and compared it with prior efforts in Figure 5.

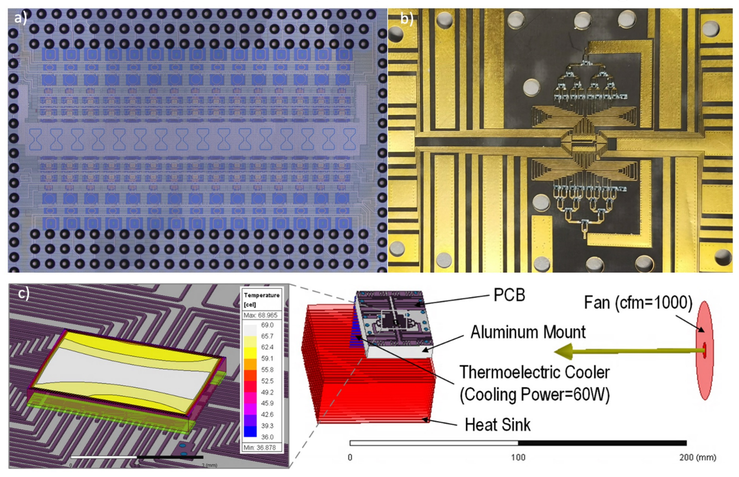

Figure 4. a) Fabricated chip die photo, b) Printed circuit board for the chip, and c) Simulated thermal performance and system design

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Publications: Jinchen Wang, Xibi Chen, Daniel Sheen, Yong Hu, Drew Michael Weninger, Yi Lin, and Ruonan Han, "A CMOS THz Source With 20dBm Radiated Power", in preparation.

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